A FLEXIBLE SPREAD SPECTRUM SYSTEM

Sidney Minard Skjei

NAVAL POSTGRADUATE SCHOOL
Monterey, California

THESIS

A FLEXIBLE SPREAD SPECTRUM SYSTEM

by

Sidney Minard Skjei, Jr.

June 1975

Thesis Advisor: J.E. Ohlson

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER	2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle)	5. TYPE OF REPORT & PERIOD COVERED
A Flexible Spread Spectrum System	Master's Thesis; June 1975
	6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s)	8. CONTRACT OR GRANT NUMBER(s)
Sidney Minard Skjei, Jr.	
9. PERFORMING ORGANIZATION NAME AND ADDRESS	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
Naval Postgraduate School Monterey, California 93940	
11. CONTROLLING OFFICE NAME AND ADDRESS	12. REPORT DATE
Naval Postgraduate School Monterey, California 93940	June 1975
	13. NUMBER OF PAGES 110
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)	15. SECURITY CLASS. (of this report) Unclassified
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Spread Spectrum
Pseudo-Noise

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A discussion of the design, and construction and utilization of a Pseudo-Noise Sequence Generator/Correlator and a Flexible Spread Spectrum System in which it is employed is presented. This equipment is an educational tool for instruction, research and demonstration of spread spectrum techniques.

Pseudo-Noise sequences of lengths 7 through 4095 are generated and utilized to spread a signal over a maximum

(20. ABSTRACT Continued)

bandwidth of approximately 15 MHz. Signals spread over a bandwidth of 5 MHz or less may be successfully recovered by means of a Delay-Lock Tracking Loop. Linear and hard-limited channel configurations are available. Message bandwidths up to approximately 28 kHz are accommodated.

While design as an educational tool, the Flexible Spread Spectrum System has a stand-alone capability as a cable communications system.

A Flexible Spread Spectrum System

by

Sidney Minard Skjei, Jr.
Lieutenant, United States Navy
B.S., United States Naval Academy, 1967

Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
June 1975

ABSTRACT

A discussion of the design, and construction and utilization of a Pseudo-Noise Sequence Generator/Correlator and a Flexible Spread Spectrum System in which it is employed is presented. This equipment is an educational tool for instruction, research and demonstration of spread spectrum techniques.

Pseudo-Noise sequences of lengths 7 through 4095 are generated and utilized to spread a signal over a maximum bandwidth of approximately 15 MHz. Signals spread over a bandwidth of 5 MHz or less may be successfully recovered by means of a Delay-Lock Tracking Loop. Linear and hard-limited channel configurations are available. Message bandwidths up to approximately 28 kHz are accommodated.

While designed as an educational tool, the Flexible Spread Spectrum System has a stand-alone capability as a cable communications system.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ACKNOWLEDGMENT

The author is very grateful to his wife, Laurie, for her assistance and forbearance.

The author would also like to express his sincere thanks and appreciation to Dr. John E. Ohlson for his advice and assistance. Profound gratitude is also expressed to Mr. Ross Seely and Mr. H.S. Chin, without whose efforts and technical expertise the Flexible Spread Spectrum System would not have been possible.

I. INTRODUCTION

A. PURPOSE OF THE THESIS

The purpose of this thesis is to present the design, construction and utilization of a Pseudo-Noise Sequence Generator/Correlator and a Flexible Spread Spectrum System in which it is employed. While this system is designed to be a versatile research tool and demonstration aid, it has a stand-alone capability as a spread spectrum cable communications system and is readily adapted to other channels.

B. SPREAD SPECTRUM COMMUNICATIONS

While sacrificing linear channel bandwidth and increasing system complexity, spread spectrum (SS) techniques permit low probability of intercept, jam resistant communications. Additional attributes of spread spectrum communications include multiplexing efficiency in a nonlinear channel, selective calling/identification, multipath protection, and accurate time of arrival measurement. Use of spread spectrum techniques is not limited to communications systems: navigation, identification, and radar systems currently benefit from spectrum spreading.

There are three primary spread spectrum techniques: pseudo-noise (PN) modulation, frequency hopping, and time hopping. Only PN modulation will be discussed since the

Flexible Spread Spectrum System (FSSS) is a PN modulated communications system. For the same reason, discussion of spread spectrum techniques will be limited to their use in communications systems.

The block diagram of a conventional communications system is shown in Figure 1, as are the frequency domain representations of signals at various points in the system Conversion of this system to a spread spectrum system is shown as Figure 2 along with the new frequency spectra. The only signal processing modifications involved in the change are: (a) modulation of the message carrying signal by a PN sequence at the transmitting and receiving terminals, and (b) a synchronization loop for the receiving terminal's PN generator. PN sequence characteristics are discussed in detail in IIA. A typical sequence is shown as Figure 7c.

A comparison of frequency spectra in Figures 1 and 2 shows that the converted system's transmitted signal has been "spread" in frequency and has a lower power spectral density; at the receiver, the message spectral density is increased to its "pre-spread" level. This spreading and despreading is made possible by the autocorrelation function exhibited by PN sequences (Figure 5). When the transmitting terminal's PN generator is clocked at a frequency (f_s) which is much greater than the message bandwidth (f_m), the message spectrum is spread to a new bandwidth approximately equal to f_s. Correspondingly, the average message power spectral

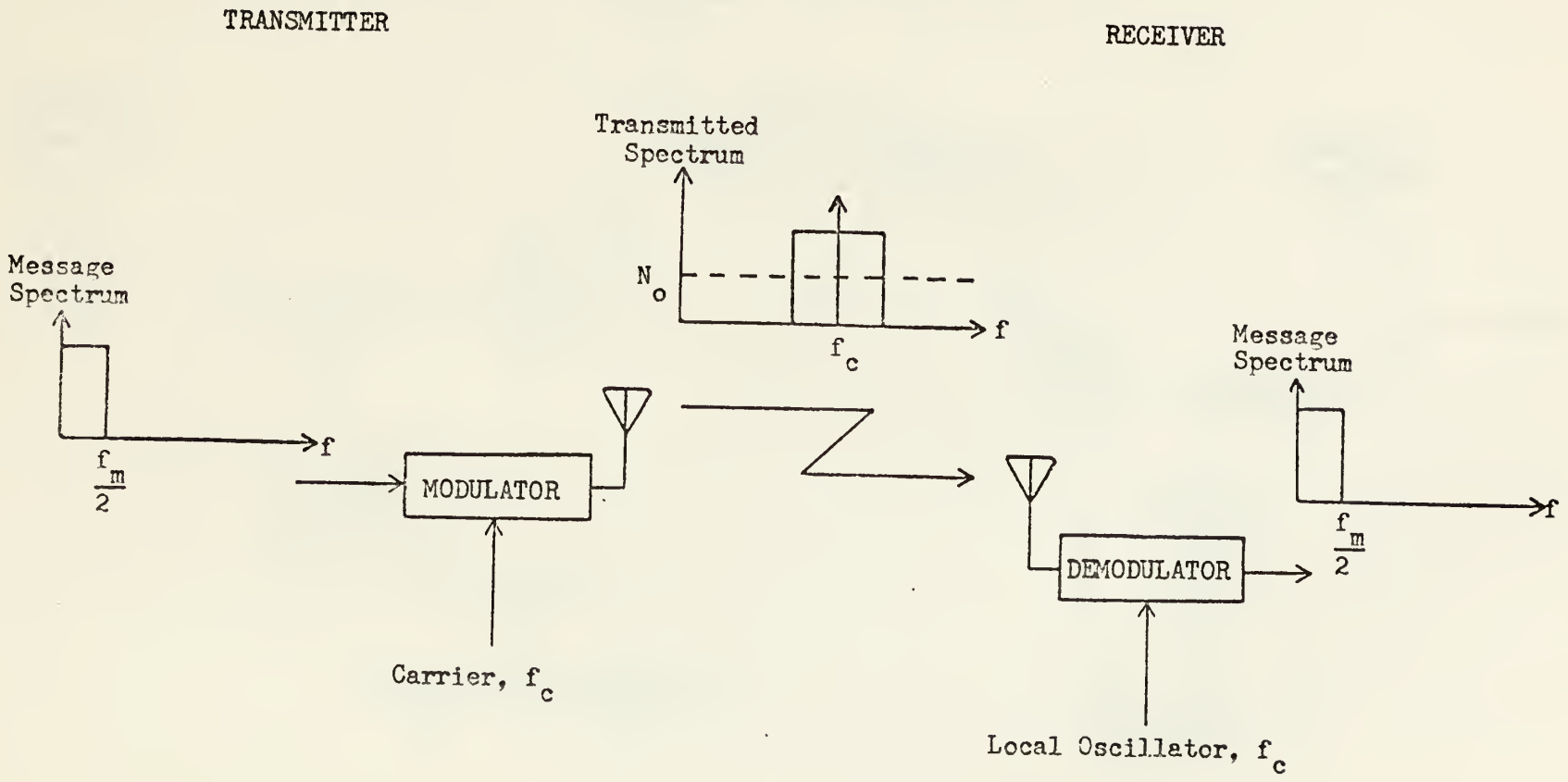


Figure 1. SIMPLIFIED BLOCK DIAGRAM OF A CONVENTIONAL COMMUNICATIONS SYSTEM

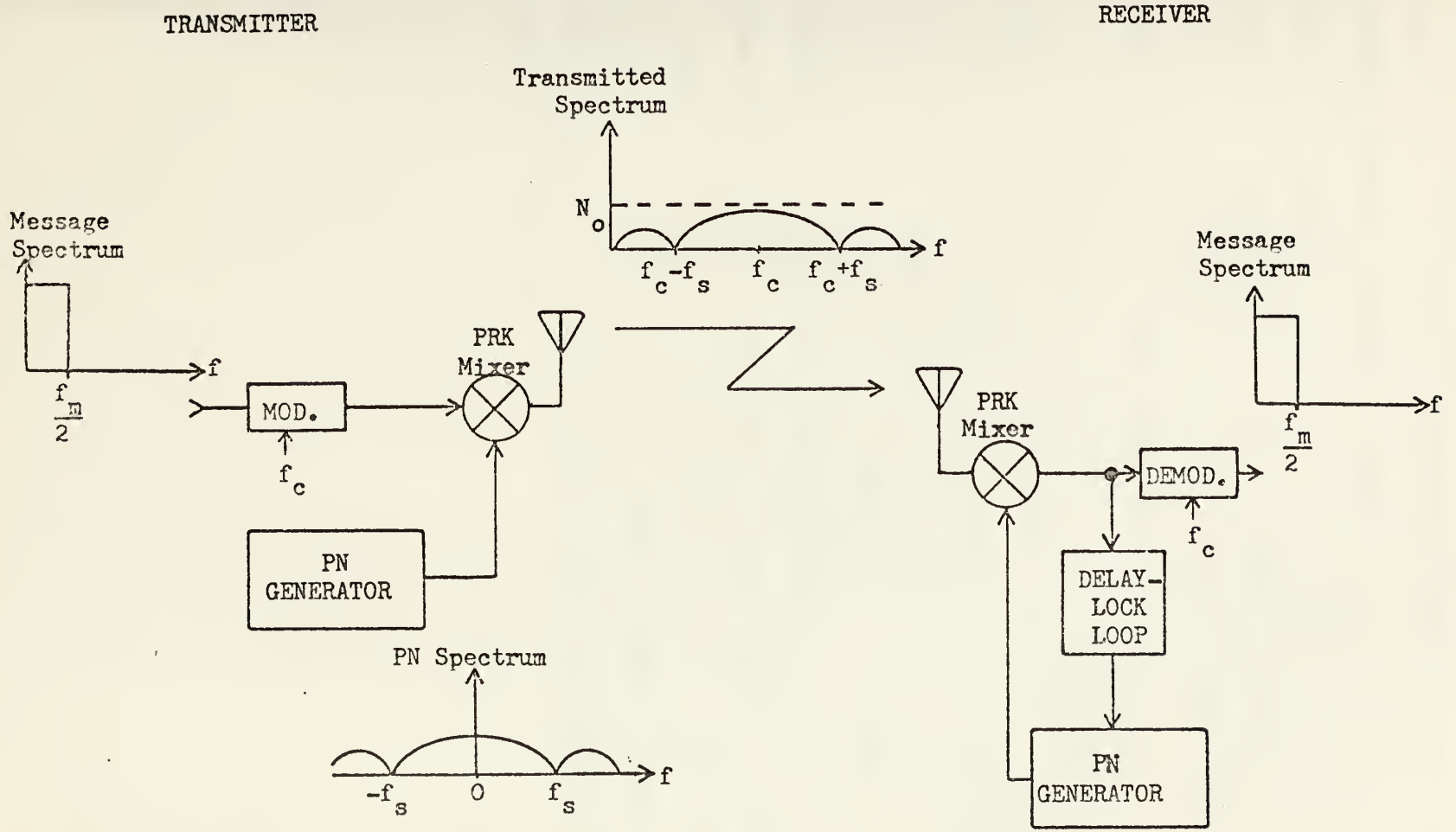


Figure 2. SIMPLIFIED BLOCK DIAGRAM OF A SPREAD SPECTRUM COMMUNICATIONS SYTEM

density is decreased by the factor f_m/f_s. This reduction results in the low probability of intercept attribute of spread spectrum systems. That is, if two stations lower their transmitted power to a level just sufficient for reliable communications, the transmitted signal's spectral density is generally below the ambient noise power spectral density N_o of an interceptor's receiver.

At the receiving terminal, code synchronization is achieved by one of several methods such as a delay-lock tracking loop, and then the receiver's PN generator despreads the desired signal while simultaneously spreading any interfering signal over a bandwidth of f_s Hertz. Since the receiver IF bandwidth is approximately f_m Hertz, the effective power of the interfering signal has been reduced by a factor of f_s/f_m. Thus, conversion of a communications system to a spread spectrum communications system decreases the probability of the system being intercepted and increases its jam resistance.

II. THE PN GENERATOR/CORRELATOR

The Flexible Spread Spectrum System includes 3 PN Generator/Correlators: one to spread the spectrum in the transmitting subsystem, another to generate a code for despreading the signal in the receiving/processing subsystem, and a third to be utilized as a co-channel user.

Each PN Generator/Correlator contains its own clock, variable length shift register, coincidence correlator, baseband delay-lock tracking loop (DLTL), and Phase Reversal Keying (PRK) modulator. Two of the PN Generators contain their own +5 and ±15 volt power supplies. A photograph of the PN Generator/Correlator is shown as Figure 3.

Although the PN Generator was designed to be a component of the FSSS it is a highly versatile unit and may be utilized in any application requiring pseudo-noise sequences or a PN PRK signal. Additionally, the PN Generator is capable of performing as a digital signal generator for a wide variety of applications.

A. PSEUDO-NOISE SEQUENCES

1. Characteristics of PN Sequences

PN sequences are repeatable binary sequences consisting of a semi-random distribution of '1's and '0's. Were their binary distribution completely random, the sequence would be non-deterministic and therefore unusable in any application requiring synchronous sequences.

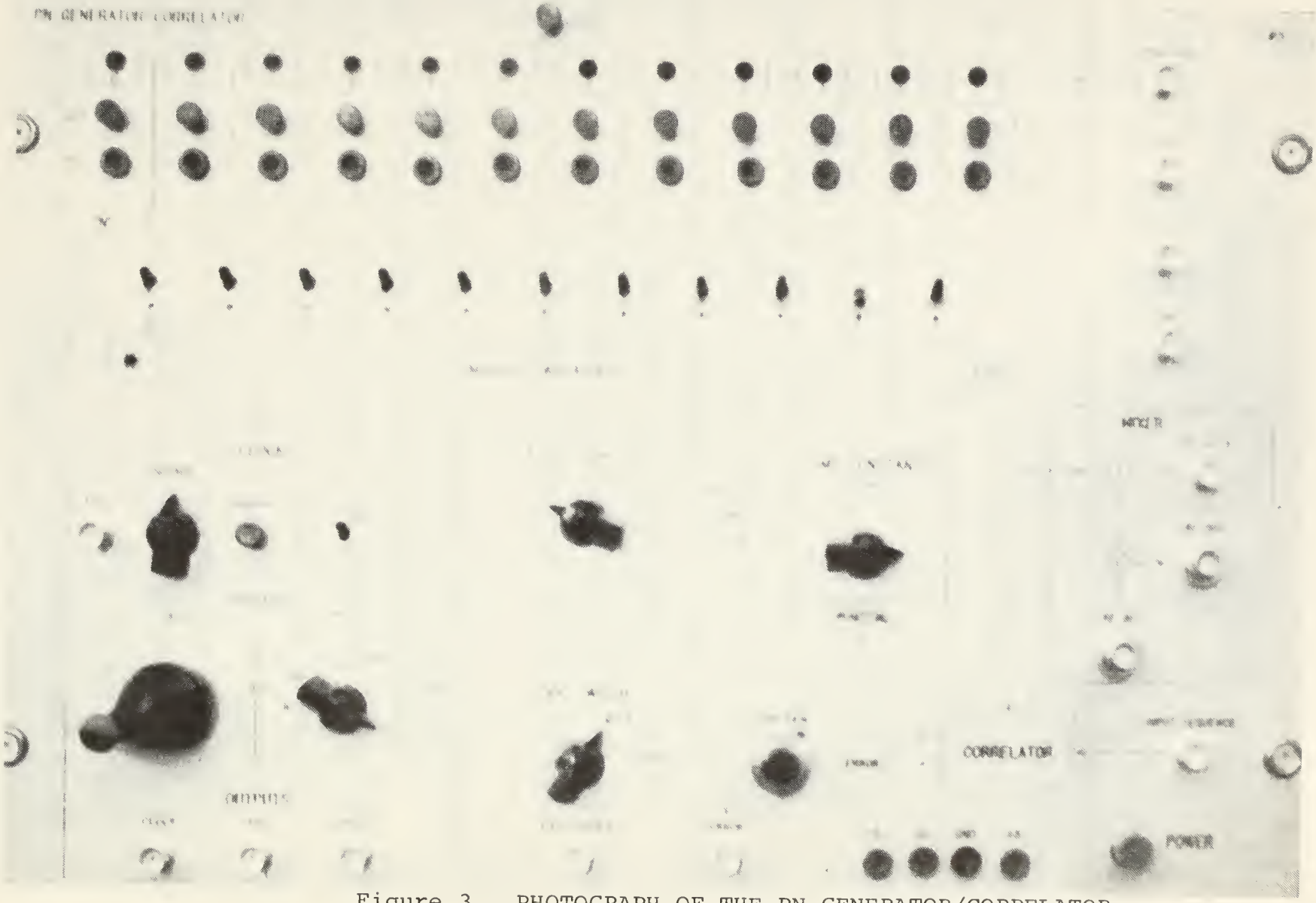


Figure 3. PHOTOGRAPH OF THE PN GENERATOR/CORRELATOR

Maximal length sequences are a particular class of PN sequences. They are typically generated by modulo-two summation and feedback of selected outputs of shift register; a typical generator is shown in Figure 4. When produced by a shift register of length "n", maximal length sequences have a period of $2^n - 1$ bits. The "-1" results from the prohibited "all 0" state: if the shift register were ever to arrive at this state, it would remain there indefinitely. As a result, the total number of '1's in a maximal length sequence is exactly one greater than the total number of '0's. In the remainder of this thesis, the terms 'maximal length sequence' and 'PN sequence' will be used synonymously.

Within a PN sequence, the proportion of "runs" of length "x", or "x" consecutive repetitions of '1's or '0's, is equal to 2^{-x}. For example, $\frac{1}{2}$ the runs are of length 1, $\frac{1}{4}$ are of length 2, etc.

The most useful characteristics of PN sequences are their cross-correlation and autocorrelation functions. Cross-correlation of a PN sequence with anything other than itself is difficult to generalize; however, it is usually significantly less than the peak of the sequence's autocorrelation function. A binary PN sequence autocorrelation function is shown as Figure 5. The value of this function for zero dislacement ($\tau = 0$) is equal to 1 and decreases to a value "y" when the displacement is greater than one bit length, T. For binary logic levels, the exact value of y is:

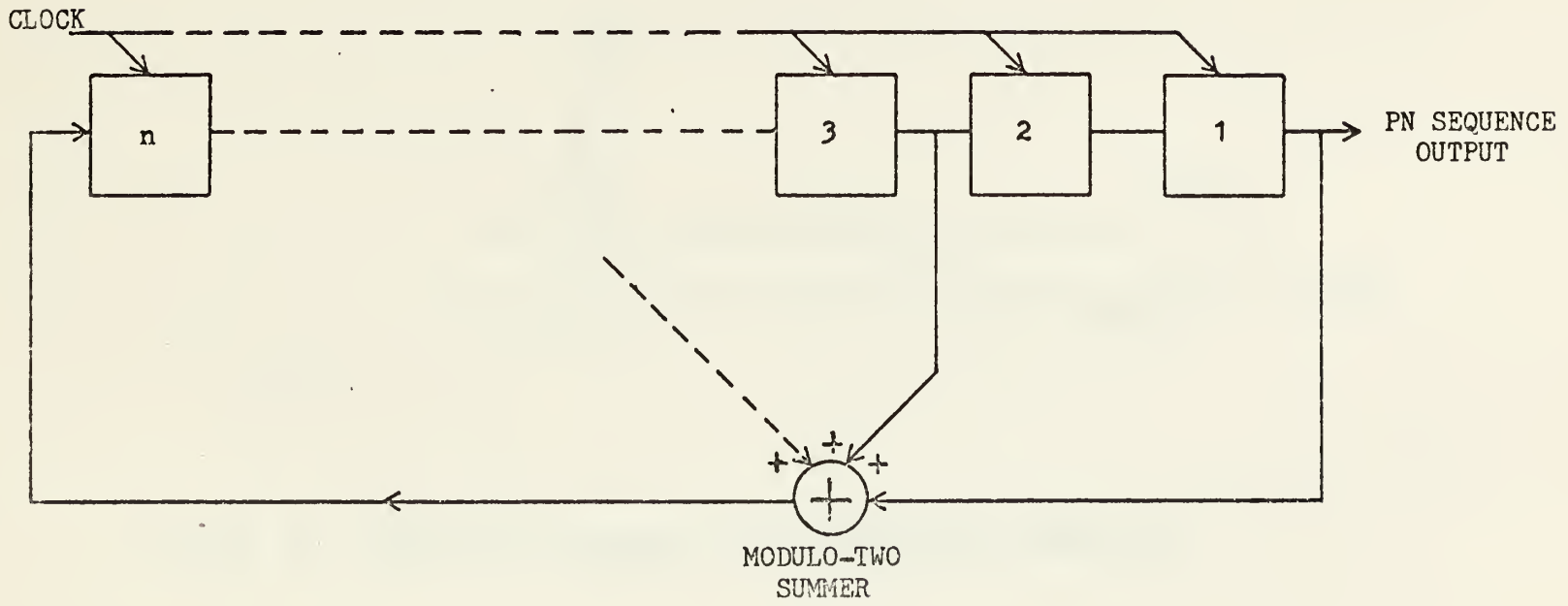


Figure 4. GENERALIZED SHIFT REGISTER PN SEQUENCE GENERATOR

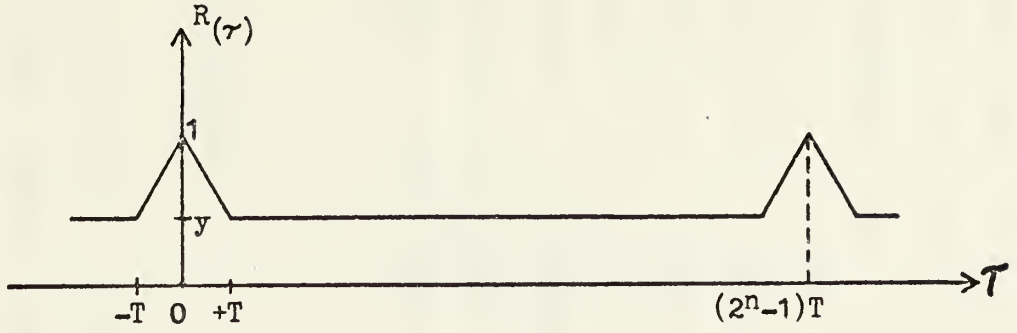


Figure 5. BINARY PN SEQUENCE AUTOCORRELATION FUNCTION

$$y = \frac{2^{(n-1)} - 1}{2^n - 1}$$

Thus, as shift register and sequence lengths are increased, y increases to a maximum value of $\frac{1}{2}$. This two level autocorrelation function recommends spread spectrum techniques for a variety of applications. In navigation and time/distance measurement applications, for example, the sharp peak of the autocorrelation function permits exact time of arrival measurement and avoidance of multipath interference by signals delayed in time by more than one bit.

Autocorrelation of a bipolar (±1) signal yields a similarly shaped autocorrelation function having a peak value of 1; however, in this case the second level of the function is:

$$y' = \frac{-1}{2^n - 1}$$

The power spectrum of a PN sequence is readily obtained by taking the Fourier transform of its autocorrelation function. Figure 6 shows the power spectrum of a PN sequence generated by a shift register of length n = 3. This spectrum consists of discrete spectral lines within an envelope E where

$$E = \left[\frac{\sin (\pi ft)}{\pi ft}\right]^2$$

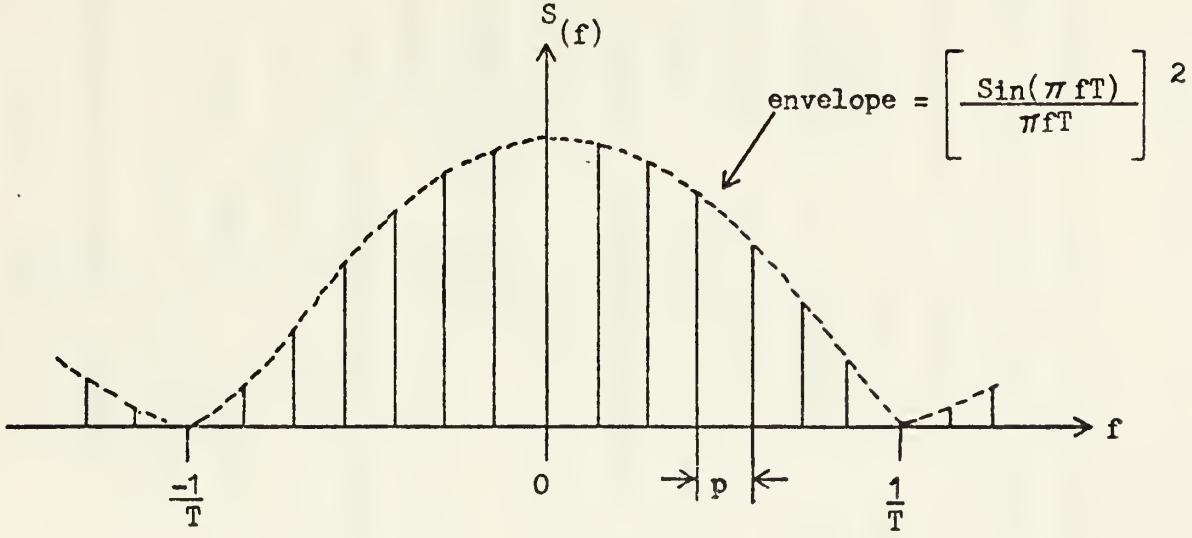


Figure 6. POWER SPECTRUM OF A PN SEQUENCE (n=3)

The separation of the spectral lines (p) within the envelope is the reciprocal of the code period, that is

$$p = \frac{1}{(2^n - 1)\ T}$$

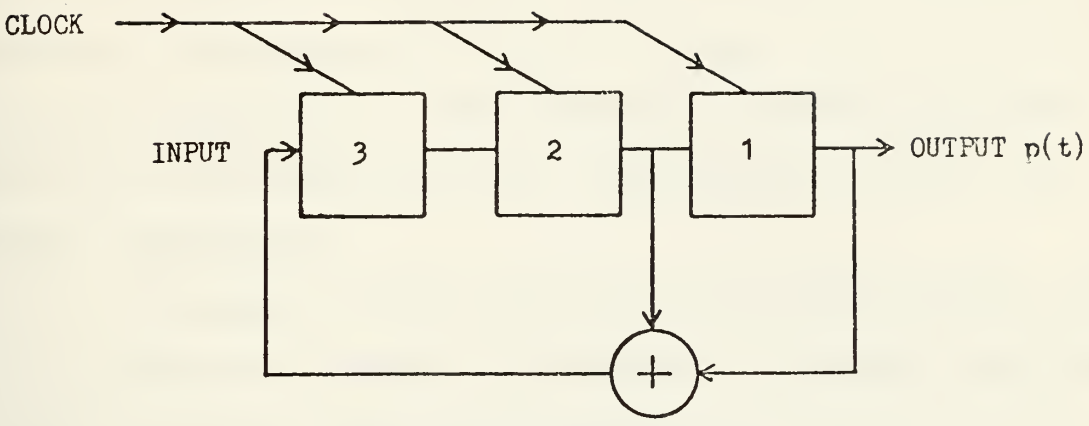
Thus, as shift register length is increased, the spectral lines become more numerous and move closer together.

At the transmitting terminal of a spread spectrum communications system (q.v. Figure 2) a modulated RF carrier is phase shift keyed by a PN sequence. This produces a signal whose spectrum, now centered at f_c, is similar to that shown in Figure 6; however, instead of discrete spectral lines, the SS signal's envelope contains replicas of the message spectrum, which are usually overlapped.

2. PN Sequence Generation

PN Sequences are generated by selectively summing the outputs of shift register positions and feeding the sum back into the shift register input. A shift register PN generator of register length 3 is shown in Figure 7a. Each time a clock pulse occurs, the outputs of register positions 1 and 2 are modulo-two summed (exclusive-or'ed) and fed back to the input of register position 3.

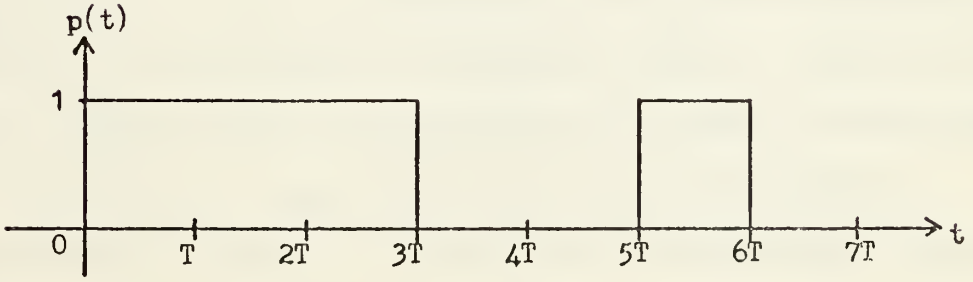
Figure 7b shows the state of the shift register flip-flops for successive clock pulses; after $2^3 - 1 = 7$ pulses the sequence repeats itself. It should be noted that the shift register takes on all possible states except



(a) Shift Register Circuit

CLOCK PULSE	REGISTER STATE
1	1 1 1
2	0 1 1
3	0 0 1
4	1 0 0
5	0 1 0
6	1 0 1
7	1 1 0
8	1 1 1

(b) Shift Register State Transition



(c) Output Pseudo-Noise Sequence

Figure 7. GENERATION OF A PSEUDO-NOISE SEQUENCE

the "000" state, a "terminal" state. Figure 7c shows the punctual PN sequence p(t) which is taken from the output of register position #1. The outputs of register positions #2 and #3 are versions of p(t) displaced by one and two bits, respectively.

Appendix B lists the various register position outputs to be modulo-two summed, or "tapped" to generate a maximal length sequence from a shift register of length 3 to 12. The mathematics for deriving codes listed in Appendix B may be found in Reference B.

3. The Delay-Lock Tracking Loop

A delay-lock tracking loop (DLTL) performs the same function for PN sequences as a phase locked loop does for sinusoids, that of bringing two signals to phase coherence. To carry the analogy further, phase detection in a phase locked loop is similar to differencing two correlation products in a DLTL.

Correlation generally consists of multiplying a signal by the delayed version of another signal (cross-correlation) or itself (autocorrelation) and integrating the result. Many types of correlators may be utilized in a DLTL, depending upon the frequency and form of the signals to be correlated. Digital correlation at baseband is accomplished by means of a coincidence correlator; Figure 8 is a block diagram of such a device. Coincidence correlators utilize the principle that modulo-two summation and inversion of binary waveforms is equivalent to multiplication.

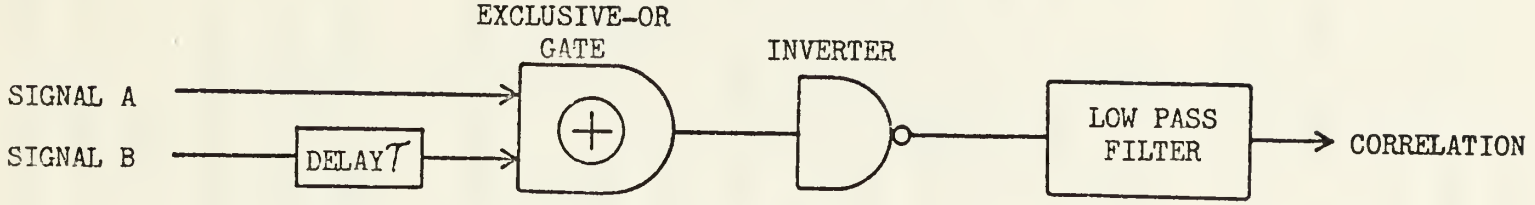


Figure 8. DIGITAL COINCIDENCE CORRELATOR

The block diagram of a DLTL is shown as Figure 9. A DLTL synchronizes two PN sequences by: (a) correlating an external sequence against 2 sequences displaced ± one bit or less from the internal sequence (b) differencing the correlation products, and (c) utilizing the resultant difference, or error signal, as a control signal for the internal sequence's Voltage Controlled Oscillator (VCO) clock.

The "early" and "late" gate signals are PN sequences displaced one bit or less in time from the reference or punctual sequence. They may be obtained from the outputs of shift register positions either side of the output, or punctual, shift register for 1 bit spacing. Thus, if register position 2 is the output register, register position number 3 is the early (E) gate and register position number 1 the late (L) gate. Normally, register position 1 is taken to be the punctual (P) position; register position 2 is then the early gate and an additional appended flip-flop is driven by register position 1 to obtain the late gate.

Figure 10 shows error signals derived from early and late signals displaced both 1 and $\frac{1}{2}$ bit from the punctual signal. The half bit error signals have twice the slope of the full bit error signals, and therefore twice the loop gain. In a first order loop, this increased gain results in half the steady state phase error as the full

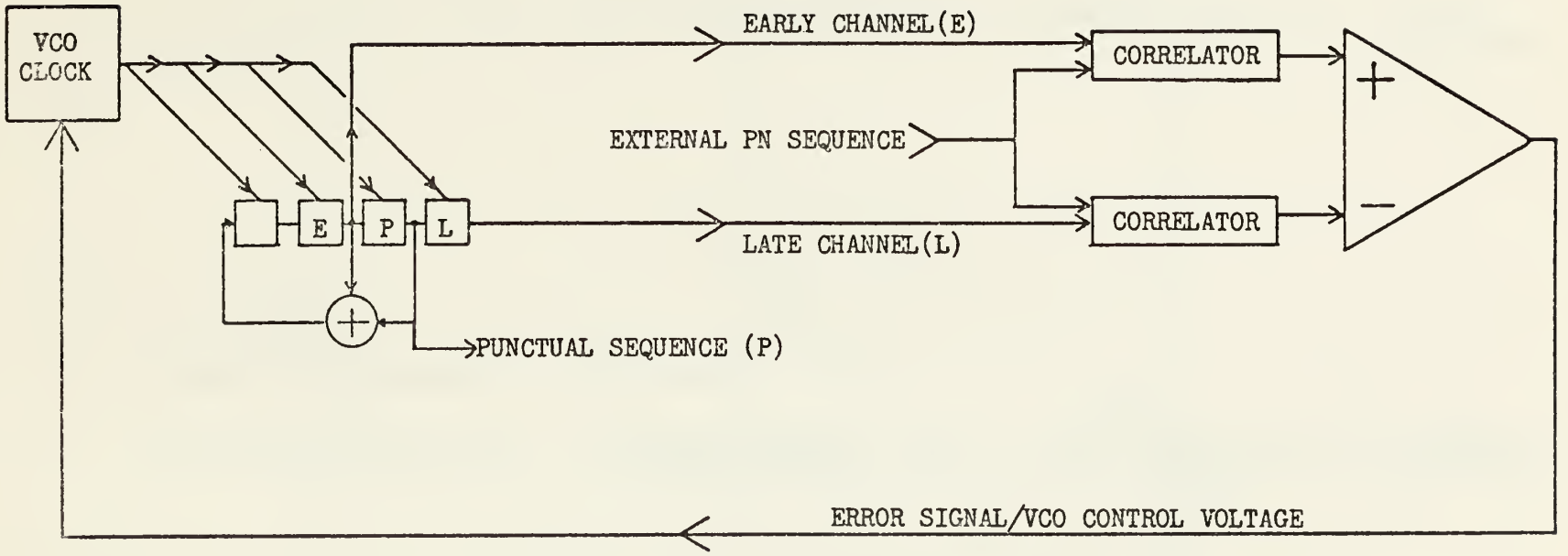


Figure 9. DELAY-LOCK TRACKING LOOP

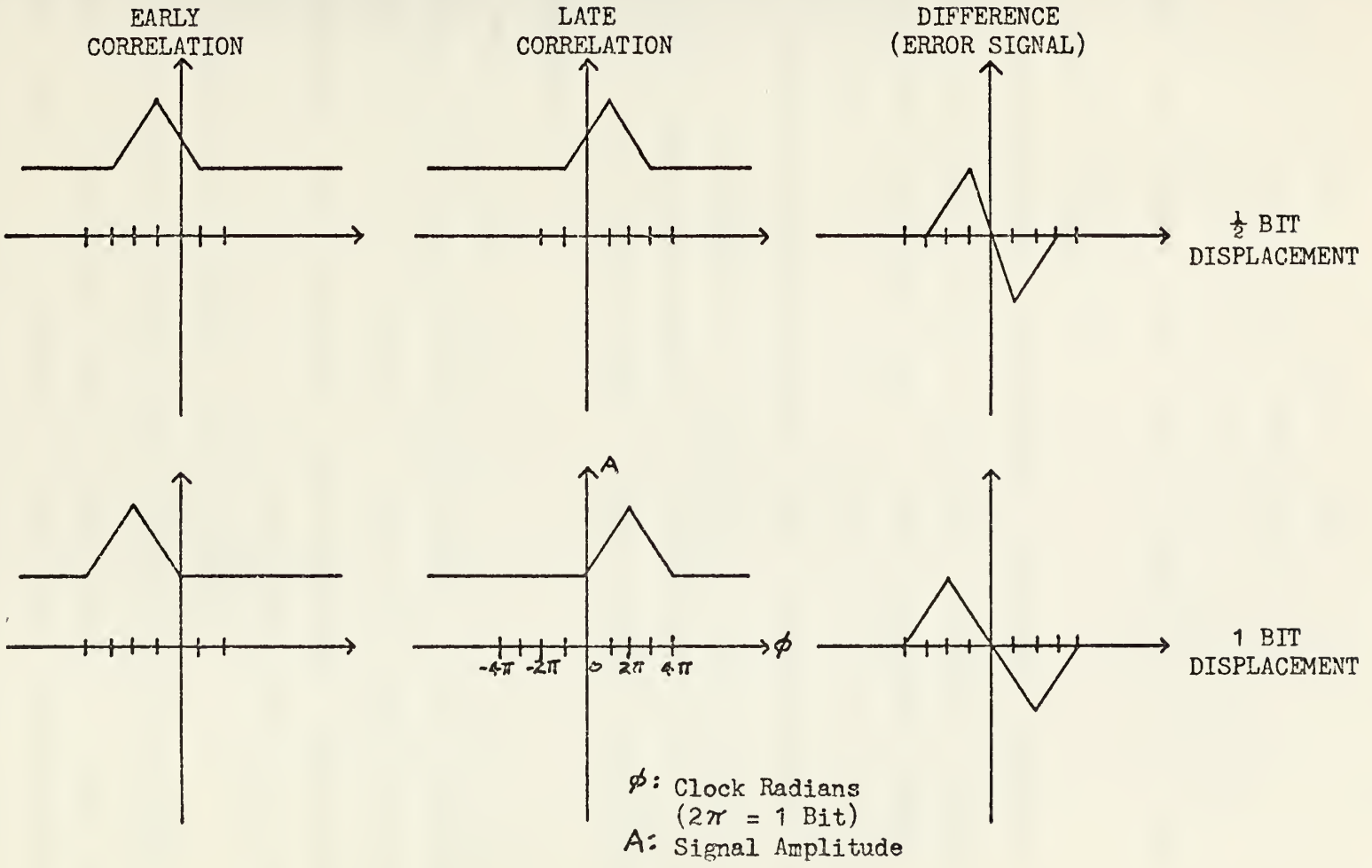


Figure 10. DELAY-LOCK TRACKING LOOP WAVEFORMS

bit error signal. Additionally, the half bit error signal has the advantage of a larger signal to noise ratio in the individual early and late channels when the loop is tracking. The full bit error signal, however, can accommodate a larger steady state phase error than the half bit error signal.

B. CIRCUIT DESCRIPTION

The PN Generator/Correlator's circuitry consists of two hard wired circuit boards, two plug in circuit boards, and a hardwired RELCOM M6A mixer. The PN generator board (abbreviated PN) is a double sided printed circuit board which generates the PN sequence and a synchronization pulse each time the sequence is repeated; it also contains line drivers capable of driving up to 20 feet of 50 or 75 Ohm coaxial cable from the EARLY, LATE, PUNCTUAL and SYNC BNC connectors.

The clock board (abbreviated CLO) is a double sided printed circuit board located parallel to the front panel at the bottom of the chassis. This board contains circuitry to generate the clock pulse, line drive the CLOCK and VCO output BNC's and provide a beat frequency difference between the internal and external clock signals.

The correlator board (abbreviated COR) is a double sided printed circuit board located perpendicular to front panel at the bottom of the chassis. This board contains control circuitry for the VCO, a coincidence correlator which

correlates the punctual signal against an external sequence and a baseband delay-lock tracking loop.

The driver board (abbreviated DRI) is single sided printed circuit board at the top of the chassis which contains buffer inverters to drive the front panel light emitting diodes (LED's) and their associated banana type jacks.

All circuit boards in the FSSS contain at least one large (2-20μf) and several small (0.01-0.1μf) supply by-pass capacitors.

1. Clock Board (CLO)

Figures 17 thru 19 contain the clock board component layout, schematic diagram, and interface diagram, respectively.

The principal component on the clock board is the voltage controlled oscillator (VCO). Specifications for this unit are listed in Table 1. Figure 11 shows a typical output frequency versus control voltage characteristic for the VCO. A manual trim control for fine adjustment of this characteristic is available on the back of the VCO.

One of three available clock modes is selected by the clock mode switch: internal clock (NORMAL), external clock (EXT), or manual clock (MAN). In NORMAL mode, the clock frequency is selected to be approximately 5, 2.5, 1 MHz, 100, 10, 1 kHz, 100, 10 or 1 Hz by utilizing the front panel frequency selector switch. Fine frequency adjustment up to 120 ppm from the selected frequency is available by rotating the "Δf" front panel handwheel knob.

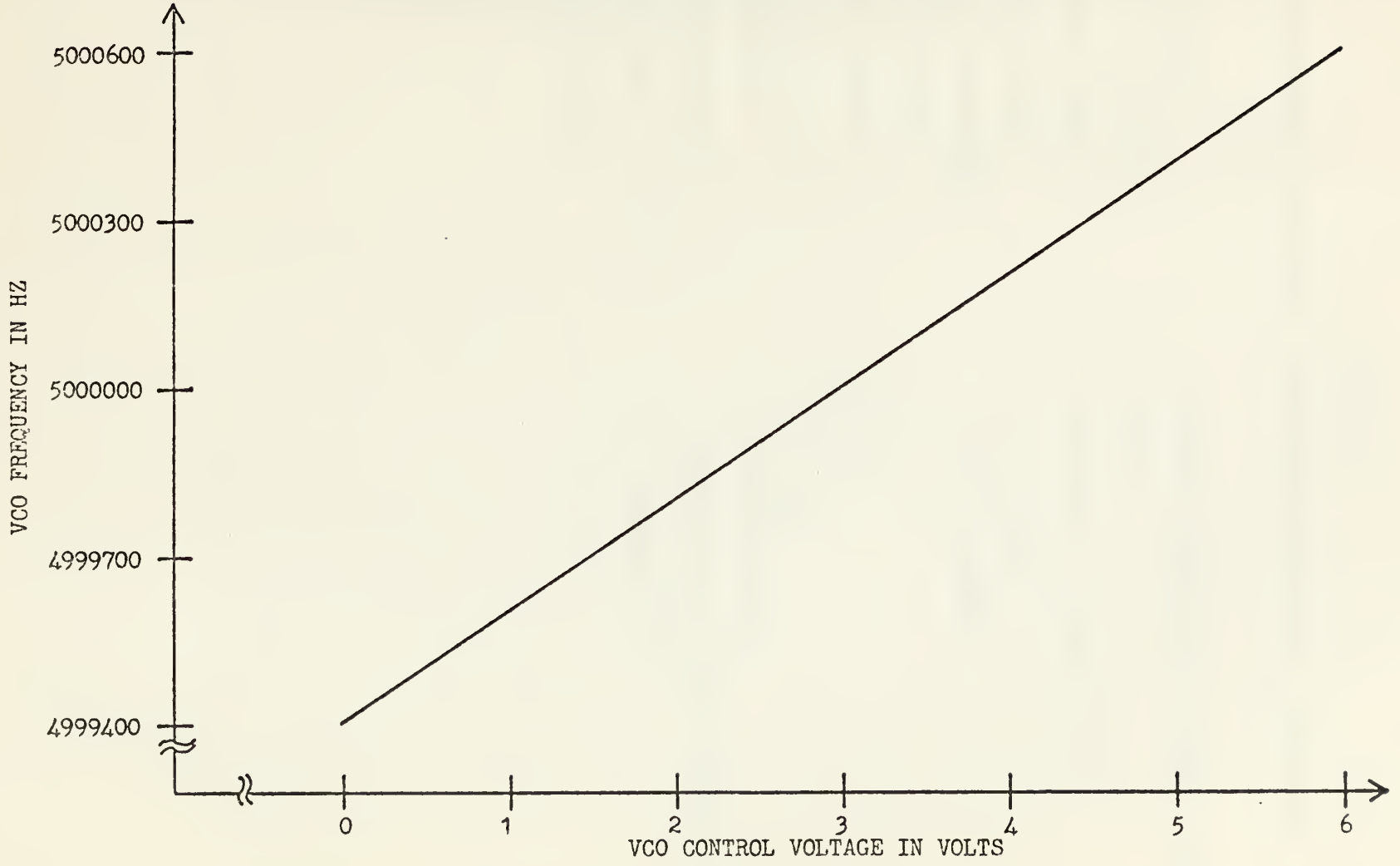


Figure 11. VCXO 255 FREQUENCY AS A FUNCTION OF CONTROL VOLTAGE

TABLE 1

SPECIFICATIONS OF VOLTAGE CONTROLLED OSCILLATOR MODEL VCXO 255

Manufacturer	Ferwalt industries, Lapwei Idaho
Center Frequency	5 Mhz
Frequency Range	4,999,400 to 5,000,700 Hz
Linearity Error	± 6% maximum
Manual Trim Range	± 50 Hz minimum
Supply Voltage	+5 v ± 3%
Supply Current	30 ma
Input Impedance	10 K ohms
Maximum Load	9 TTL load units
Output Waveform	3 v minimum peak-peak square wave
Stability 0° to 75° C.	± 200 Hz maximum
Control Voltage	0 v to +6 v

The front panel frequency selector switch consists of two wafers. The first distributes the selected frequency to the clock mode switch; the second switches a control signal to disable all divide-by-ten counters (N7490) not in use. This control arrangement reduces noise in the clock board and suppresses unwanted harmonics in the clock signal. Figure 20 shows a truth table and connection diagram for the divide-by-ten counters. The count mode is enabled by a logical 0 (ground) to $R_9(2)$ and disabled by a logical 1 (+5 v.).

IC 207 is utilized in the divide-by-five mode to produce the 1 MHz signal from the 5 MHz signal. IC's 208 thru 213 are all utilized in the divide-by-ten mode to obtain the 100 kHz thru 1 Hz signals. The 2.5 MHz clock is produced by a "t" flip-flop (IC 206) which divides the VCO output by 2. It should be noted that the 2.5 MHz clock is not further divided down; this necessitates inclusion of a switching diode on the frequency selector switch for the 2.5 MHz control signal to suppress generation of both the 2.5 and 1 MHz signals when a 5 MHz clock is selected.

A signal present at the external clock (EXT) BNC is buffered (IC 204) and distributed to both the clock frequency differencing circuitry and the external clock (EXT) position of the front panel clock mode switch.

The manual clock, IC 202, consists of a pair of NAND gates in an RS flip-flop configuration. 'Reset' and

'set' lines are connected to a pushbutton adjacent to the clock mode switch.

From the clock mode switch, the selected clock is distributed to both PN and clock boards. The clock signal is buffered and line driven to the CLOCK BNC by IC 201 on the clock board. The undivided VCO output is also line driven to the VCO BNC by IC 202.

The beat frequency between internal and external clocks (PN codes' slip rate) is produced from these two signals by modulo-two summation in IC 204, inversion in IC 202 and two stages of low pass RC filter. This signal is available at the front panel OFFSET BNC.

A "clock stop" control is effected by a front panel toggle switch connected to an RS flip-flop. The flip-flop output gates the VCO signal in IC 205. Only the internal clock is able to be stopped by means of the clock ON/STOP switch.

2. PN Generator Board (PN)

Component layout for the PN board is shown in Figure 21; functional/schematic diagrams are shown as Figures 22 thru 24. An interface diagram is shown in Figure 25.

The PN generator board contains a variable (3-12) length shift register and circuitry which generates a synchronization pulse. The sync pulse is produced when all shift register positions (flip-flops) in use are in the logical 1 state; this occurs once in each sequence period.

Analysis of the PN board circuitry is best accomplished by example. Therefore, a sample situation follows: shift register length 5, register positions 1 and 3 are modulo-two summed (tapped) and fed back to the input of register position 5. Reference to previously mentioned diagrams will assist in circuit analysis.

Wafer #1 of the REGISTER LENGTH switch distributes the output of the modulo-two adder; wafer #2 switches a sync pulse control voltage. The modulo-two sum of flip-flops #1 and #3 is sent to PN-R5 via wafer #1. This is a 'special' wafer: unselected positions are tied together and grounded. As a result, J12, R11 thru R6, R4 and R3 receive a logical 0. Since J12 is logical 0, Q12 is 0, $\overline{Q}12$ is 1. When $\overline{Q}12$ is exclusive-or gated (IC 181) with R11 (logical 0), the result is that J11 receives a logical 0. In like manner, K11 receives logical 1. Flip-flop 11 therefore emulates flip-flop 12 and outputs (Q11) logical 0. This "daisy chain" operation progresses with each clock pulse. After 6 clock pulses, Q6 becomes logical 0, $\overline{Q}6$ logical 1. When these two signals are separately exclusive-or gated (IC 184) with R5 (output of modulo two adder), J5 receives the output of the modulo-two adder and K5 receives the inverted output. The preceeding steps may be summarized as follows: when register length "n" is selected, register positions "n+1" thru 12 are forced to maintain a logical 0 state and the modulo-two adder output is switched and gated into the input of register position "n".

Q5 and $\overline{Q5}$ are now separately exclusive-or gated with R4 (logical 0) and their respective modulo-two sums are sent to J4 and K4; however, since the modulo-two sum of any logic level "A" with 0 is always "A", Q5 and $\overline{Q}5$ are effectively directly transferred into J4 and K4, respectively. This gating is continued between register positions 4 and 3; from this point on, each flip-flop output is hardwired into the input of the next flip-flop.

The Boolean algebra expressions for the input to the 'k'th flip-flop is:

$$J_k = Q_{k+1} \oplus P$$

$$12 \geq k \geq 3$$

$$K_k = \overline{Q}_{k+1} \oplus P$$

$$J_k = Q_{k+1}$$

$$3 \geq k \geq 1$$

$$K_k = \overline{Q}_{k+1}$$

where P is the control/signal from wafer #1 of the REGISTER LENGTH switch such that

P = (output of modulo-two adder), if register length K is selected

= 0 , otherwise

Analysis by example of the sync pulse generating circuitry proceeds in a similar manner. Wafer #2 of the REGISTER LENGTH switch distributes a +5 v. (logical 1) signal to PN-5; PN-12 thru PN-6 and PN-4 receive a logical 0 from this wafer. $\overline{Q}12$, previously shown to be logical 1, is NAND gated with PN-12 (logical 0) in IC 101; the output of this gate (logical 1) is sent to the sync pulse generating AND gates. These AND gates produce a sync pulse when all their inputs are logical 1. NAND gates associated with register positions 11 thru 6 output logical 1 for reasons identical to those described above for register position 12.

Since wafer #2 of the REGISTER LENGTH switch sends a logical 1 to PN-5, both OR gate outputs in IC 113 are logical 1. In general, the output of the 'n'th OR gate is sent to the input of the 'n-1'th OR gate. Therefore, logical 1 is NAND gated with the $\overline{Q}$ outputs of flip-flops 5 and 4; when the latter are logical 0, the NAND gate outputs are logical 1, which is sent to the sync pulse generating AND gates. The Q outputs of register positions 3 thru 1 are hardwired to these same AND gates (IC's 121 and 122).

In summary, when register length 5 is selected, NAND gates associated with register positions 12 thru 6 are forced to the logical 1 state by wafer #2 of the REGISTER LENGTH switch. When flip-flops 5 and 4 are logical 1, all NAND gates send logical 1 to the sync pulse generating AND gates. When flip-flops 3 thru 1 are also logical 1, all AND gate inputs are logical 1 and a sync pulse is generated.

The Boolean Algebra expression for the sync pulse, S, is

$$S = Q3 \cdot Q2 \cdot Q1 \cdot \left[\prod_{n=4}^{12} \overline{Q}_n \cdot (R_n + R_{n+1} + R_{n+2} + \ldots + R_{12}) \right]$$

where R is the control voltage from wafer #2 of the REGISTER LENGTH switch such that

$R_n = 1$, if register length 'n' is selected

$R_n = 0$, otherwise.

The PN board contains two 74S140 line drivers (IC's 140, 141) capable of driving coaxial cable from the PUNCTUAL, EARLY, LATE and SYNC BNC connectors located on the front panel. An appended flip-flop (IC 177) which is driven by the punctual (#1) register position produces the LATE signal.

IC 191, the modulo-two summer, is a Fairchild 9348 dual in-line package (DIP) 12 input parity checker. The outputs of this device consist of odd parity and even parity signals. The odd parity signal (PN-PO) is connected to wafer #1 of the REGISTER LENGTH switch; the even parity output is inverted (IC 104) to drive the front panel LED which indicates the status of the modulo-two adder.

The clock signal from the clock mode switch is buffered by two levels of inverters (IC 104) in order to increase fan out while preserving phase. The first level consists of one inverter; the second consists of two inverters driven by the first level. Each second level inverter drives approximately half the flip-flops' clock inputs.

3. Correlator Board (COR)

The component layout for the correlator board is shown in Figure 26; a circuitry diagram is shown as Figure 27 and an interface diagram in Figure 28.

The correlator board makes extensive use of the type 5558 linear integrated circuit; this device consists of two operational amplifiers (OP AMPS) in an 8 pin DIP. These devices are utilized for all OP AMP applications on the correlator board, including unity gain voltage followers used to buffer all analog inputs and outputs.

The correlator board contains a delay-lock tracking loop, punctual signal coincidence correlator, VCO control signal circuitry and RELCOM M6A mixer drive circuitry.

The punctual signal coincidence correlator and DLTL circuitry consists of IC's 31 thru 33 and their associated components. Early, punctual and late signals are simultaneously coincidence correlated with the signal (normally another PN sequence) present at the input sequence BNC; this operation consists of modulo-two summation (IC 31)

followed by inversion (IC 32) and integration. More specifically, inverted early, punctual and late signals are correlated with the inverted input sequence BNC's signal; however, since

$$X \oplus Y = \overline{X} \oplus \overline{Y},$$

inversion prior to coincidence correlation has no effect on the correlator output.

Early and late correlator integration is accomplished by means of fixed value low pass filters (R301,302; C31,32) whose time constant is 0.1 ms. Punctual correlator integration time constants of approximately 1000, 100, 10, 1, 0.1 or 0.01 milliseconds may be selected at the front panel TIME CONSTANT switch; this switch varies the shunt capacitance of a single low pass RC filter. The TIME CONSTANT switch also includes a "0" position, selection of which results in no correlator integration.

The punctual coincidence correlation signal is available at the front panel CORRELATION BNC. Early and late coincidence correlation signals are differenced in IC 33 to obtain the DLTL 'error' signal. This signal is then buffered to the LOOP GAIN potentiometer. The center tap of this 20 K Ohm potentiometer is buffered to both the ERROR BNC and the LOOP SWITCH. When the LOOP SWITCH is in the CLOSED position, the DLTL error signal is added (IC 34) to

the VCO quiescent bias (2 - 4 volts dc) produced by the front panel Δf potentiometer. Any signal present at the EXTERNAL CONTROL BNC is also added to the VCO control signal in IC 34.

The RELCOM M6A double balanced mixer drive circuitry consists of an exclusive-or gate, an inverter, and two switching transistors. The exclusive-or gate modulo-two adds the punctual signal to any message signal present at the TTL DATA BNC; the gate then drives a single transistor directly and one after inversion. The transistor output signals are each connected to one of the mixer's "I" ports; a logical 1 exclusive-or gate output results in current being driven through the mixer's I ports in one direction, a logical 0 results in current being driven through in the opposite direction. When the current drive through the I port is reversed, the carrier signal present at the mixer's "L" port is phase shifted 180 degrees, resulting in Phase Reversal Keying (PRK).

4. Driver Board (DRI)

The driver board contains four N7404 hex inverters which drive the register position LED's and banana type plugs. The $\overline{Q}$ output of each register position flip-flop on the PN board is distributed to two inverters on the driver board: one drives an LED, the other drives a banana plug. Figures 29 and 30 show component layout and circuitry for this board.

C. OPERATING THE PN GENERATOR

1. Front Panel Description

a. Light Emitting Diodes

LED's indicate the state of a particular register position or the modulo-two adder. A lighted LED indicates the logical 1 state.

b. Pushbuttons

(1) Clear. The CLEAR pushbutton clears all register positions but does not clear the appended 'late' flip-flop discussed in B.2.

(2) Set. These pushbuttons are utilized to individually set a particular register position flip-flop.

(3) Manual Clock. When the clock mode switch is in the MAN position, the manual clock pushbutton controls the clock state.

c. Toggle Switches

(1) Register Position Tap Switches. These toggle switches are utilized to connect a particular register position output to a modulo-two adder input port.

(2) Clock Stop. This switch may be used to stop the internal clock and thereby discontinue generation of the PN sequence when the clock mode switch is in the NORMAL position. When switched to the STOP position, this switch also stops the CLOCK BNC output.

d. Rotary Switches

(1) Register Length Switch. The REGISTER LENGTH switch controls the length (n) of the shift register generating the PN sequence. Register lengths 3 thru 12 are available.

(2) Clock Mode Switch. This switch selects either an external (EXT) clock, internal (NORMAL) clock, or manual (MAN) clock.

(3) Frequency Selector Switch. When the clock mode switch is in the NORMAL position, the frequency selector switch controls the approximate (± 120 ppm) clock frequency.

(4) Time Constant Switch. This switch is utilized to either vary the integration time constant of the punctual signal correlator, or eliminate correlator integration altogether (0 position).

(5) Loop Switch. When the LOOP SWITCH is in the CLOSED position, the DLTL error signal is switched into (added to) the VCO control signal.

e. BNC Connectors

(1) Punctual BNC. The PUNCTUAL BNC contains the line driven output of the punctual (#1) register position.

(2) Early BNC. The line driven output of the early (#2) register position is available at the EARLY BNC.

(3) Late BNC. This BNC connector outputs the line driven late gate flip-flop's signal.

(4) Sync BNC. The line driven synchronization pulse is available at this BNC connector. This signal should be utilized to externally trigger any oscilloscope used to display the PN sequence.

(5) RF In BNC. This BNC is utilized to connect a carrier frequency input to the L port of the RELCOM M6A mixer. It should be noted that the 1 dB compression point of the M6A mixer is 2 dBm (for its 50 Ohm impedance).

(6) TTL Data BNC. This connector is used to input phase shift keying message (data) modulation; the modulation input signal must be TTL compatible (0-4 v. levels). Input impedance of this connector is that of a standard TTL gate.

(7) RF Out BNC. This output contains the modulated signal produced by phase shift keying the RF IN BNC's signal by the modulo-two sum of the punctual PN sequence and the TTL DATA input.

(8) Input Sequence BNC. This BNC is utilized to provide an input (normally another PN sequence) to the coincidence correlator and delay-lock tracking loop. This input is internally terminated in 50 Ohms in PN Gen. #2 and #3.

(9) Error BNC. The delay-lock tracking loop output, level controlled by the GAIN potentiometer, is present at this BNC connector.

(10) Correlation BNC. This output contains the coincidence correlation of the signal present at the INPUT SEQUENCE BNC and the punctual signal; correlator integration time constant is controlled by the TIME CONSTANT switch.

(11) External Control BNC. This BNC provides a 1 MΩ impedance input port for an external VCO control signal (0 to ± 3 v. level).

(12) Clock BNC. The line driven clock output is available at this BNC connector.

(13) VCO BNC. This BNC contains the line driven VCO output; this signal is not influenced by any gating or switching circuitry.

(14) Offset BNC. This output contains the frequency difference between the signal present at the EXT BNC and the internal clock. It has a dc component so a counter should be used on "pulse" input.

(15) EXT BNC. A 0 to 15 MHz TTL compatible signal present at this input becomes the shift register clock when the clock mode switch is in the EXT position. This connector is internally terminated in 50 Ohms.

f. Banana Jacks

(1) ± 15. These banana jacks provide ±15 volt tracking power supply outputs (@ 150 ma); they should not be used separately.

(2) +5. This TTL compatible 5 volt power supply output is capable of providing up to 1.5 amperes to an external load.

(3) Gnd. The common and chassis ground for all power supplies and signals is available at the GND banana jack.

(4) Register Position Banana Jacks. These banana jacks contain the register position flip-flop outputs.

g. Potentiometers

(1) Gain Potentiometer. This potentiometer controls the magnitude of the delay-lock tracking loop error signal.

(2) Δf Potentiometer. This potentiometer permits continuous frequency variation of the internally generated clock within limits of ± 120 ppm.

h. Push-Push Switch

The POWER switch controls distribution of 120 v. ac to all power supplies. The switch light is lighted by the +5 v. power supply. On PN Generator/Correlator #2 this device is utilized only as an indicator of available +5 v. power, since an external master switch controls power to the unit.

2. Generating a PN Sequence

To generate a PN sequence and display it on an oscilloscope, the following procedure should be followed.

a. Turn POWER on; power light should be visible.

b. Set clock mode switch to desired clock source and set clock ON/STOP switch to the ON position.

c. If NORMAL clock mode is selected, set desired clock frequency at the frequency selector switch. Set Δf potentiometer handwheel knob to mid-range.

d. Turn REGISTER LENGTH rotary switch to desired register length.

e. Set tap toggle switches for the particular PN generating code to be used to the IN position. A full listing of all usable codes is contained in Appendix B; a partial listing is given in Table 2.

f. If clock frequency is 100 Hz or greater, all selected register position LED's will be lit. If all LED's are dark, the register may be "stuck" in the 'all 0' state; to remedy this condition, push the SET pushbutton on register position #1.

g. A PN sequence should now be ready for display. Connect the PUNCTUAL BNC output to one channel of an oscilloscope; externally trigger the oscilloscope with the output of the SYNC BNC. Ensure that all oscilloscope inputs are terminated in 50 Ohms.

3. Operating the Coincidence Correlator and DLTL

To synchronize PN sequence 'B' with PN sequence 'A' and observe their punctual coincidence correlation (utilizing PN Generator/Correlator 'B') the following procedure should be followed. Note: Terminate oscilloscope, frequency counter, and PN Gen #1 INPUTE SEQUENCE BNC in 50 Ohms.

TABLE 2

SUMMARY OF PN SEQUENCE GENERATING CODES

Register Length 'n'	Total Codes Available	Sample Codes*
2	Not available with PN Generator	
3	2	(2)**, (3)**
4	2	(2)**, (4)
5	6	(3)**, (4)
6	6	(2)**, (6)
7	18	(2)**,(7),(5)
8	16	(3,4,5),(5,6,7)
9	48	(5), (6)
10	60	(4), (8)
11	176	(3)**,(10)
12	144	(4,10,11),(2,5,7)

NOTE: *To generate a PN Sequence by a particular length shift register, switch the below listed TAP switches ( ) to the IN position. Reference to Figure 4. will assist in switch identification.

**Utilizing these codes, the PN Generator/Correlator is capable of producing PN sequences at clock frequencies up to 15 MHz, if an external clock is used.

a. Following the procedure listed in II.C.2 above, generate two PN codes of similar clock frequency, register length and code.

b. Connect PN Generator/Correlator 'A's PUNCTUAL BNC output into PN Generator/Correlator 'B's INPUT SEQUENCE BNC and channel #1 of a dual trace oscilloscope. Utilize 'A's SYNC BNC output to externally trigger the oscilloscope.

c. Connect PN Generator/Correlator 'B's PUNCTUAL BNC output to channel #2 of the oscilloscope: sequence 'B' should now be visible 'slipping' past a stationary sequence 'A'.

d. To determine sequence slip rate (clock beat frequency) connect PN Gen. 'A's CLOCK BNC output to PN Gen. 'B's EXT BNC input; slip rate may now be obtained by connecting PN Gen. 'B's OFFSET BNC to a frequency counter.

e. To synchronize the sequences turn 'B's LOOP SWITCH to the CLOSED position. After a maximum period of time equal to the sequence length (in bits) divided by the slip rate (in Hz), both codes should appear stationary and within one bit period of time synchronization. However, if the sequences do not 'lock up', increase 'B's LOOP GAIN potentiometer setting and/or adjust its Δf potentiometer to decrease slip rate. Given maximum loop gain, sequences should lock for slip rates less than 400 Hz.

f. To observe either punctual coincidence correlation or the DLTL error signal, connect the CORRELATION or

ERROR BNC's to an oscilloscope, unlock the loop, and slip the sequences at maximum slip rate by setting 'A's Δf potentiometer fully clockwise, and 'B's fully counter-clockwise.

4. Generating a Spread Spectrum Signal

a. Set up a PN Generator/Correlator to generate a PN sequence as described above.

b. Utilizing a good quality RF signal generator, adjust (modulated) carrier power output to 0 dBM (50 kHz to 200 MHz) for optimum mixer performance.

c. Connect (modulated) carrier signal to PN Gen.'s RF IN BNC input. The output spread signal should now be available at the RF OUT BNC.

d. To add PSK message modulation, connect a TTL compatible message data signal to the TTL DATA BNC input. The signal at the RF OUT BNC will now be bi-phase modulated with the modulo-two sum of the PN sequence and the message data signal.

D. TROUBLESHOOTING THE PN GENERATOR

Since the PN Generator/Correlator performs a limited number of specific functions, it is possible to classify any circuitry failure by the affected functional area; i.e. the PN Gen. will not clock, or it will not produce a sync pulse, etc. Therefore, the subject of troubleshooting the PN Gen. will be categorized into failures in primary functional areas: clock, sequence, and sync pulse generation and delay-lock loop tracking.

1. Clock Failures

Failures in clock signal generating circuitry are easily recognized: the state of the PN Generator/Correlator stays fixed when it should be constantly changing. The logical troubleshooting procedure in this case is to start with the VCO output and trace the clock signal through to the PN board. The following procedure is offered as the most expeditious means of diagnosing a particular clock circuitry failure.

a. Connect the VCO BNC output to an oscilloscope terminated in 50 Ohms; a square wave of approximately 0 to 4 volts should appear which has a period of 200 ns. If this signal is observed, proceed; if it is not, check the clock board to ensure that the VCO is properly connected to +5 volts and ground, and that the VCO output is not shorted.

b. Set the Frequency Selector Switch to the 5 MHz position. Connect the CLOCK BNC output to an oscilloscope terminated in 50 Ohms and verify that the presentation is the same as observed in (a) above. If the presentation is different, a fault probably exists in IC's 204, 205, or 206, or their interconnecting switch wiring. Check the CLOCK ON/STOP switch to ensure that it is in the ON position and that pins 11 and 12 of IC 206 are at ground and +5 v. potentials.

c. Subsequent troubleshooting steps are iterative in nature due to the fact that generation of a particular clock frequency consists of dividing the next higher frequency. The only exceptions to this rule are the 2.5 and 1 MHz clock frequencies, both of which are obtained from the 5 MHz VCO. If the 10 kHz output is inoperative, for example, the 1 kHz output should be checked. If no problem is found with the 1 kHz signal, the casualty is probably in the frequency selector switch wiring, because IC 210 is receiving the correct 10 kHz signal. On the other hand, if the 1 kHz output is also inoperative, the fault is associated with IC 209, the divide-by-ten counter which divides the 100 kHz signal to obtain the 10 kHz signal. Figure 20, the divide-by-ten counter detail, shows the correct control voltages for divide-by-ten operation.

2. PN Sequence and Sync Pulse Failures

PN sequence and sync pulse failures are easily confused. Therefore, when either failure is suspected, the same procedure should be followed. Connect a VTVM to the SYNC BNC output and set the CLOCK ON/STOP toggle switch to STOP. Turn the REGISTER LENGTH SWITCH to '12' and SET all register positions. As each register position is set, note the VTVM reading: only when all positions are set should the indication change from 0 to 4 volts. Repeat this procedure for register lengths 11 thru 3; this verifies

that a sync pulse is generated only when all register positions are logical 1. It is now possible to check out the PN sequence generating circuitry.

a. With the clock still stopped and the REGISTER LENGTH switch set to '12', SET all register positions and switch all taps to the OUT position. The LED on the modulo-two adder should now be dark, indicating a modulo-two sum of 0. Now successively switch all taps to the IN position, noting the LED on the adder: when an even number of taps are thrown, the LED should be dark, when an odd number are thrown, the LED should light. If this test is not successful, there is a fault with the modulo-two adder, IC 191, or with its associated tap switches.

b. With the clock mode switch set to the MAN position, CLEAR all register positions and switch all taps to the OUT position; SET one of the register positions. Manually clock the shift register by pushing the MAN pushbutton. The lighted LED should be observed to progress through the shift register; if this does not occur, note the register position at which an anomaly takes place. The casualty lies in that flip-flop or in its associated gating and switching circuitry.

c. Switch the clock mode switch to the NORMAL position and STOP the clock; select a clock frequency of 1 kHz or more. Set the REGISTER LENGTH switch to '12' and CLEAR the register. Now switch the clock ON; no change

should occur in the register - all LED's should remain dark. Repeat this procedure for register lengths 11 thru 3. This is a second check of the register position flip-flops and their associated gating and switching circuitry.

3. Delay-Lock Tracking Loop Failures

When any failure in the correlator board is suspected, the PN Gen. should be turned off and the clock board removed. This is done to protect the VCO against a control voltage in excess of 6 volts. While there are Zener diodes on both correlator and clock boards to act as voltage limiters for the control voltage, they should not be relied upon. After removing the clock board, connect a VTVM to COR-1 and set its scale to 0 - +10v. Terminate the INPUT SEQUENCE BNC with a 50 Ohm load and set the LOOP GAIN potentiometer to the fully clockwise (maximum gain) position.

a. With the LOOP SWITCH in the OPEN position, CLEAR the shift register and set the state of register position #2 equal to the LATE BNC output. The VTVM reading should be adjusted to 3 v. by adjusting the Δf potentiometer. If this is not possible, there is a fault in IC 34 or 35/ associated components.

b. CLOSE the loop switch; the VTVM reading should not change by more than 0.5 volts. If the reading on the VTVM exceeds 4. volts, and both early and late gates are in the logical 0 state, a casualty in the 'early' signal path, or IC 33 is indicated. If the VTVM reading drops

below 2 volts, a casualty is indicated in the 'late' signal path or IC 33. If both early and late gates are in the logical 1 state, opposite casualties are indicated.

III. THE FLEXIBLE SPREAD SPECTRUM SYSTEM

A. SYSTEM CHARACTERISTICS AND CONFIGURATIONS

Because the FSSS was designed to be a research and instruction tool, its primary attribute is versatility. Either linear or hard limiting channels may be simulated; channel signal to noise ratio is continuously variable. Five monitor points are available throughout the system for classroom demonstration purposes. A PSK modulator and AM demodulator are built into the system, and a frequency modulator is available. PSK and FM demodulators are planned additions.

The FSSS is divided into transmitting, receiving, and processing subsystems; however, this division is more a matter of physical proximity than simulation of a particular link. The transmitting subsystem consists of two PN Generator/Correlators, #1 and #3.

The receiving subsystem, shown in block diagram form of Figure 12, is mounted on a 19" cabinet panel. A photograph of the receiving subsystem is shown as Figure 13. This subsystem contains components which adjust the system signal to noise ratio and determine channel characteristics. Noise power is provided by a noise source capable of delivering up to -45 dBm of approximately white noise in a 10 MHz bandwidth centered at 30 MHz: the approximate passbands of the IF and hard limiting amplifiers. A coaxial switch selects the output of either amplifier.

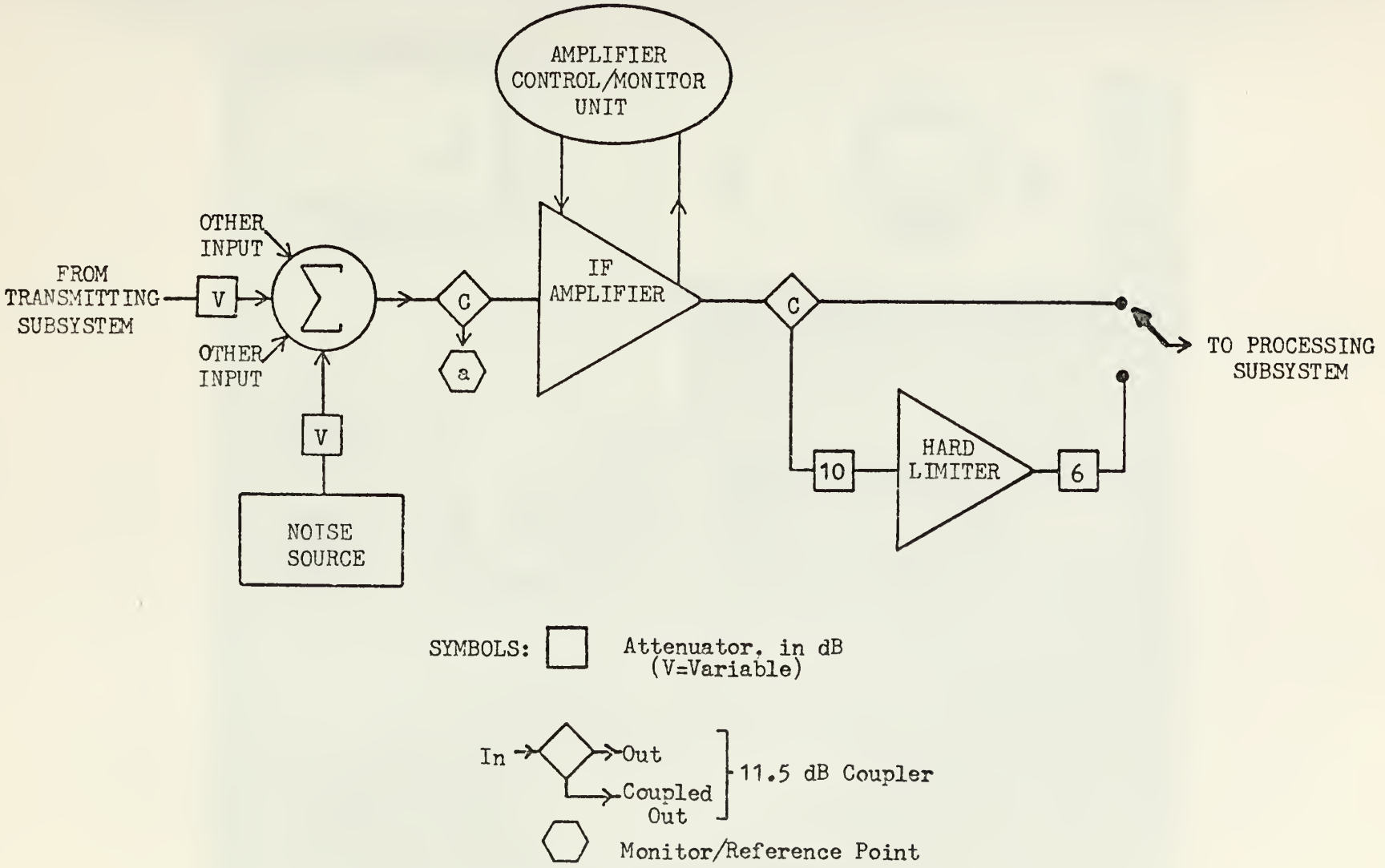


Figure 12. BLOCK DIAGRAM OF THE RECEIVING SUBSYSTEM

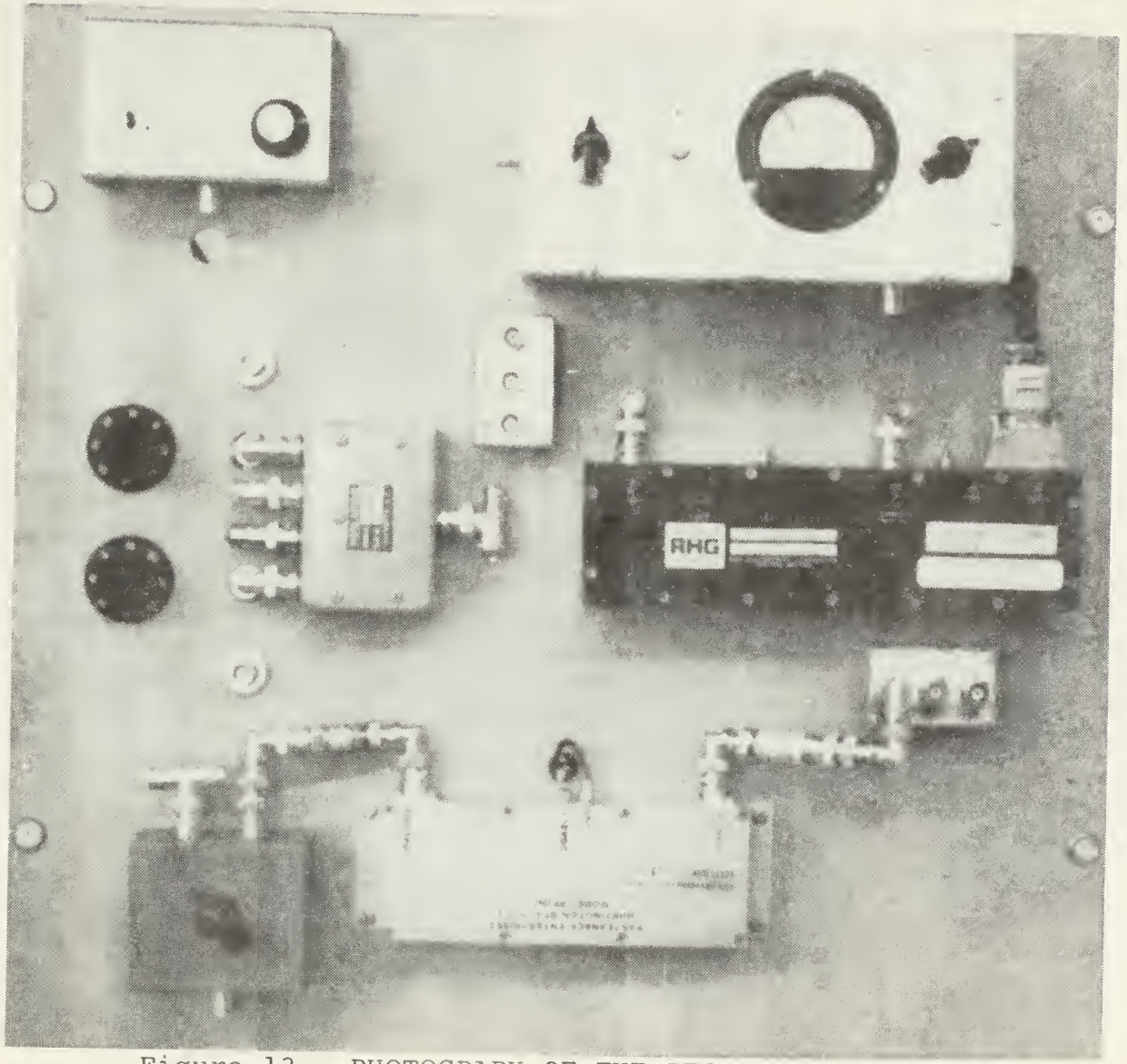


Figure 13. PHOTOGRAPH OF THE RECEIVING SUBSYSTEM

A panel meter located in the IF Amplifier Control/Monitor Unit permits measurement of either IF amplifier video output or gain control voltage. This unit is also used to select the source of IF amplifier gain control voltage: AGC, MGC, or external gain control. The IF Amplifier should normally be operated in the AGC mode with output level fixed at 1 dBm. In order to minimize system level changes when switching amplifiers, the 7 dBm output of the hard limiter is attenuated by 6 dB.

The processing subsystem is shown in block diagram form as Figure 14. A photograph of this subsystem is shown as Figure 15. The processing subsystem is also mounted on a 19" cabinet panel and may be functionally subdivided into the punctual channel correlator and the delay-lock tracking loop.

A signal input to the processing subsystem is correlated with early, punctual and late signals from the processing PN Generator/Correlator. Correlation is accomplished by means of RELCOM M6A mixers followed by bandpass filters. After filtering, all correlation products are envelope detected; punctual correlation is then available for demodulation. Early and late channel correlation products are differenced and fed back as a control voltage for the processing PN Gen, forming a delay-lock tracking loop.

The displacement of the early and late signals from the punctual signal may be selected to be either $\frac{1}{2}$ or 1 bit period by utilizing the "$\frac{1}{2}$ - 1 bit switch".

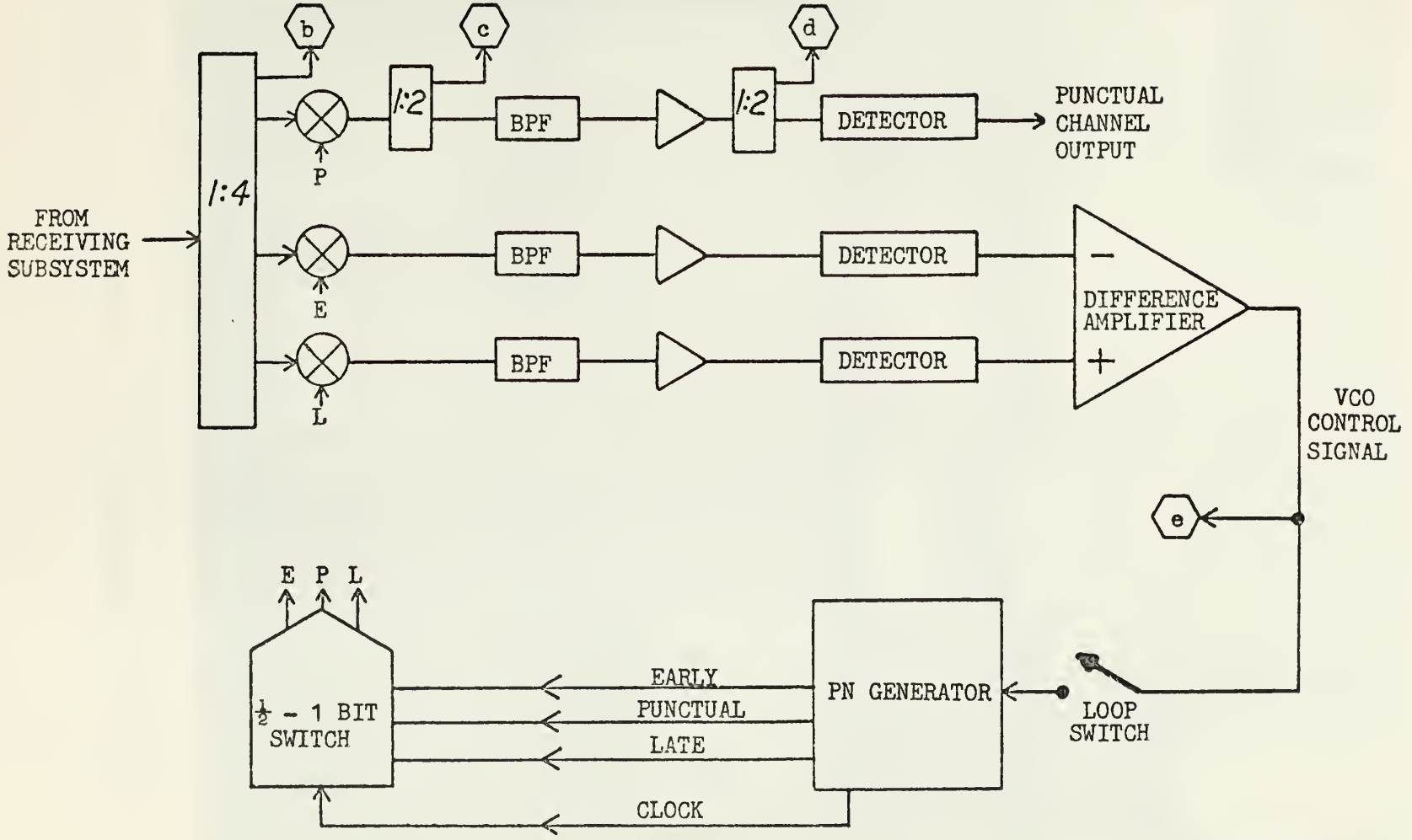


Figure 14. BLOCK DIAGRAM OF THE PROCESSING SUBSYSTEM

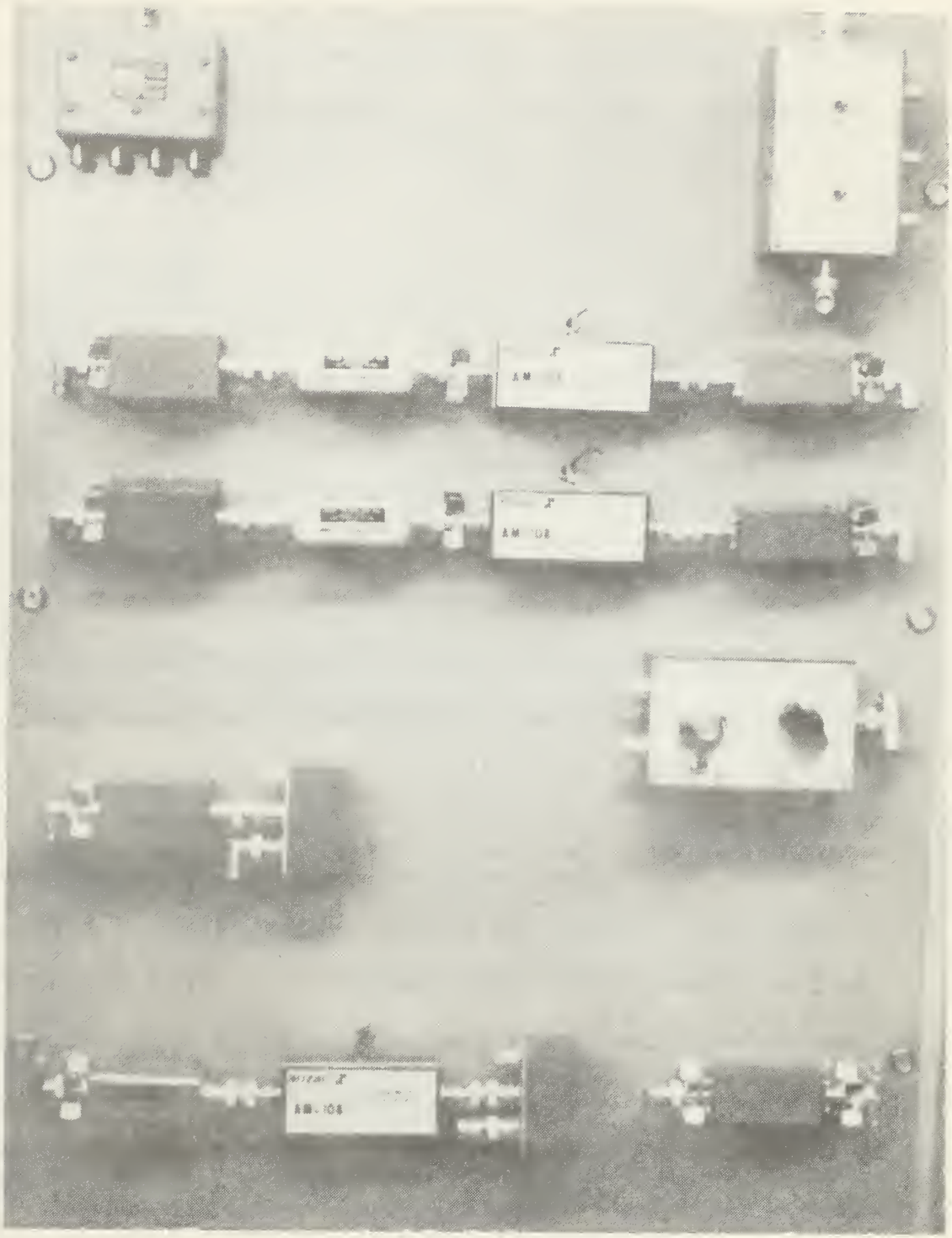


Figure 15. PHOTOGRAPH OF THE PROCESSING SUBSYSTEM

Due to the narrow bandwidth of the bandpass monolithic crystal filters, the largest message bandwidth which the system can faithfully accommodate is approximately 28 kHz. Referring back to paragraph I.B. the system processing gain, G_p, is defined as:

$$G_p = \frac{f_s}{f_m}$$

For the case of a 28 kHz message bandwidth and a 5 MHz clock frequency, the system processing gain is 22 dB. If a smaller message bandwidth is utilized, and the tracking loop bandwidth is reduced by decreasing the loop gain (reducing the gain of the processing subsystem difference amplifier), a greater system processing gain may be realized.

The FSSS is easily converted from a SS communications system to a conventional communications system. Switching the CLOCK ON/STOP switches on the transmitting and processing PN Generators to the STOP position immediately stops all spreading and despreading action by stopping the shift register clocks. This action effectively removes all PN Generators from the system, due to the "balanced" nature of the RELCOM M6A mixers. When current is constant through the mixer 'I' port in either direction, the RF signal present at the 'L' port is passed to the 'R' port with minimum attenuation and either 0 or 180 degrees phase shift.

B. OPERATING THE FLEXIBLE SPREAD SPECTRUM SYSTEM

1. Transmitting Subsystem

For system operation with an AM or FM modem, a modulated RF signal is provided to the FSSS by an RF signal generator such as a HP 8640B. The modulated carrier, at a level of 0 dBm, is connected to the RF IN BNC connector on the transmitting subsystem PN Generator; this level assures optimum mixer performance. For PSK system operation, an unmodulated carrier is connected to the RF IN BNC connector; the TTL compatible message data, at a data rate less than 20 kilobits per second, is connected to the TTL DATA BNC connector. Clock frequency, register length and code are set and the modulated spread waveform is available at the RF OUT BNC connector. This signal is then connected to a variable attenuator adjacent to the receiving subsystem 4 way combiner.

2. Receiving Subsystem

a. Input Power Levels

Input signal and noise power levels at the receiving subsystem are controlled by two variable attenuators. Two other input signals, such as a jammer or another spread spectrum signal may be added without variable attenuation. Typical system power levels for threshold, average, and strong signal cases, measured at monitor points a, b, and d, are listed as Table 3. This table includes minimum and maximum values of signal and noise power measured at monitor point (a), the 11.5 dB down coupled input to the

TABLE 3

SYSTEM OPERATING LEVELS WITH IF AMPLIFIER
AGC SET FOR 1.0 dBM OUTPUT POWER

Monitor Point and Parameter	Threshold Case	Strong Signal Case	Average Case
(a) Coupled input to IF Amplifier			
Signal			
Max:	-27 dBm	-10 dBm	-13 dBm
Min:	-110 dBm	-93 dBm	-96 dBm
Noise			
Max:	-10 dBm	-16 dBm	-13 dBm
Min:	-93 dBm	-99 dBm	-96 dBm
SNR:	-17 dB	6 dB	0 dB
(b) Input to Correlating Mixers			
Signal:	-24 dBm	- 7 dBm	-10 dBm
Noise:	- 7 dBm	-13 dBm	-10 dBm
(c) Amplified Filter Output			
Signal:	- 6 dBm	10 dBm	8 dBm
Noise:	-15 dBm	-22 dBm	-18 dBm
SNR:	9 dB	32 dB	26 dB

IF Amplifier. To obtain the actual input signal and noise power into the IF Amplifier, add 11.5 dB to values measured at monitor point (a). Signal and noise power levels may be adjusted separately utilizing a spectrum analyzer or vector voltmeter, then combined to give the desired signal to noise ratio.

b. Gain Control

Gain control of the IF Amplifier is selected and adjusted by utilizing the Amplifier Control/Monitor Unit. This unit enables selection of either automatic gain control (AGC), manual gain control (MGC), or external gain control (0 to -4.5 v.). A variable potentiometer is provided for varying the MGC voltage. The panel meter on the Amplifier Control/Monitor Unit provides an indication of either gain control voltage or detected output power (2 scales).

Automatic gain control utilizes a 15 microsecond time constant and is therefore unsuitable for AM signals. For AM operation, select MGC and set the detected output voltage level at 2v. corresponding to 1 dBm output power. AGC should be utilized and a 20 dB attenuator placed between the IF Amplifier and its input to the Amplifier Selector Switch.

c. Amplifier Selection

Selection of either the Hard Limiter or the IF Amplifier is accomplished by the Amplifier Selection Switch. While values listed in Table 3 are for the IF Amplifier,

there is less than 2 dB variation when the hard limiting amplifier is utilized.

3. Processing Subsystem

a. Processing PN Generator/Correlator

The processing PN Generator should be set for similar register length, clock frequency, and code as the transmitting PN Generator. The processing PN Gen. LOOP SWITCH is set to the OPEN position to avoid unwanted VCO biasing. If desired, the transmitting PM Gen. clock signal may be connected to the EXT BNC input of the processing Gen; code slip rate may then be measured by connecting the OFFSET BNC to a frequency counter.

b. $\frac{1}{2}$ - 1 Bit Switch

This switch has two controls; a punctual channel stop switch used to stop the punctual channel despreading, and a $\frac{1}{2}$ - 1 bit switch. The latter varies the tracking loop error signal by displacing the early and late channels either $\frac{1}{2}$ or 1 bit period from the punctual channel. These different error signals are shown in Figure 10. This switch affects the gain of the DLTL. Normally it will be placed in the $\frac{1}{2}$ bit position; this provides early and late channels with a sufficient signal to noise ratio when the loop is locked and tracking. If the 1 bit switch is selected, early and late channels are constantly differencing noise and more phase jitter is observed.

c. Difference Amplifier

There are three controls on the early/late channel differencing amplifier: the LOOP switch, GAIN potentiometer, and GAIN toggle switch. The LOOP switch is either opened or closed, depending upon whether acquisition and tracking are desired. The setting of the loop switch has no influence on the reference point (e) monitor signal.

The loop gain toggle switch selects either a maximum gain of 3 (LOW position) or 23 (HIGH position). This switch should be set to the lowest level consistent with satisfactory loop tracking performance to prevent saturation of the amplifier.

The loop GAIN potentiometer continuously varies loop gain within the LOW or HIGH range selected by the loop GAIN toggle switch. This potentiometer should also be set to the lowest possible level to ensure the minimum essential loop bandwidth.

C. DESCRIPTION OF SPECIFIC SYSTEM COMPONENTS

1. Amplifiers and Amplifier Control

a. RHG IF Amplifier

Specifications of the RHG model EST 3010 IF Amplifier are listed in Table 4; a pin connection diagram is given as Figure 31. This amplifier outputs an internally generated AGC voltage and has inputs for AGC and MGC control

TABLE 4

AMPLIFIER SPECIFICATIONS

AMPLIFIER:	IF AMPLIFIER	HARD LIMITER	CHANNEL AMPLIFIERS
MANUFACTURER:	RHG Electronics Inc.	Pasternack Enterprise	Anzac Electronics
MODEL NUMBER:	EST 3010	PE 1142	AM-108
CENTER FREQUENCY:	30 MHz	30 MHz	
3 dB BANDWIDTH:	12.5 MHz	10 MHz	400 MHz
MAXIMUM POWER GAIN:	83 dB	37 dB	28 dB
OUTPUT:	20 dBm	7 dBm	15 dBm @ -15 v. supply voltage
1 dB COMPRESSION POINT:	15 dBm		13 dBm @ -15 v. supply voltage
NOISE FIGURE:	1.5 dB		5.2 dB
POWER SUPPLY:	+12 v. @ 200 ma. -12 v. @ 40 ma.	-12 v. @ 50 ma	-15 v.
TERMINATIONS:	50 Ohms	50 Ohms	50 Ohms
MINIMUM INPUT POWER LEVEL:	-85 dBm	-30 dBm	
AGC TIME CONSTANT:	15 micro sec.		
VOLTAGE REQUIRED FOR 60 dB of MGC RANGE:	-4.3 volts dc		
AGC COMPRESSION RATIO:	60 dB/3 dB		

signals. However, the MGC input is not utilized in the FSSS application: all gain control voltages are brought into the AGC input connection, after appropriate current limiting. The amplifier has three signal ports: IF in, IF out, and video out. The video output is capable of 5 v of detected output into a 93 Ohm load and is utilized as an indication of amplifier output power. A 'DC SET' potentiometer is available on the amplifier to adjust the bias of the video output (0 - 2.5 v dc). The AGC DELAY potentiometer located on the amplifier sets the AGC controlled output power level; this control will normally be set for 1 dBm output power. A GAIN potentiometer is also located on the amplifier to limit the maximum available amplifier gain. A biasing potentiometer is located inside the amplifier which compensates for offsets in the AGC difference amplifier.

b. Amplifier Control/Monitor Unit

A schematic diagram of the Amplifier Control/Monitor Unit is shown as Figure 32. This unit is utilized to select the gain control voltage source, vary the MGC voltage level, and provide a measure of either gain control voltage or video output. Two scales of video output level are available: 0 - 1 volt and 0 - 10 volt.

c. Hard Limiter

The specifications for the Pasternack model PE 1142 Hard Limiter are listed in Table 4. The input power range of this unit is from -30 dBm to 0 dBm; thus, the output

of the IF Amplifier, coupled down 11.5 dB and attenuated 10 dB, can never exceed the maximum input level of the hard limiter. On the other hand, if the output of the IF Amplifier drops below -10 dBm, sufficient power is not available to ensure proper operation of the hard limiter; this situation can be corrected by removal of the 10 dB attenuator at the Hard Limiter input port.

d. ANZAC Channel Amplifiers

Three ANZAC amplifiers are utilized in the punctual, early, and late channels; their specifications are listed in Table 4. These amplifiers may be provided with -15 to -25 v supply voltage. In order to minimize power supply requirements and provide protection to the point contact diode detectors, these amplifiers are supplied with -15 volts; increasing the supply to -25 volts, however, will raise the 1 dB compression point from 15 to 19 dBm. The gain characteristics of these amplifiers have been matched to their particular channel; therefore, they should not be interchanged.

e. Difference Amplifier

A circuit diagram for the Difference Amplifier/ Loop Switch unit is shown as Figure 33. Operation of this unit is described in III.B.3. This amplifier consists of a two stage difference amplifier utilizing Burr Borwn 3522K operational amplifiers: each stage is operated in inverting

mode and is separately adjustable for offset voltage. This unit requires ± 15 v supply voltages.

2. Noise Source

The noise source located in the receiving subsystem simulates ambient noise at the receiver or satellite transponder. It is capable of delivering -46 dBm of approximately white noise into a 10 MHz bandwidth centered about 30 MHz. This device is compatible with 50 Ohm coaxial cable. A schematic diagram for this unit is shown as Figure 34. The noise generating element for this device is an SR 1410-70 Noise Diode; this diode produces optimum noise characteristics when back-biased by approximately 18 volts. Following the noise diode are two stages of common emitter and one stage of emitter follower transistor amplifiers. Ten decibels of LEVEL control are achieved by varying the feedback of the output stage to the emitter resistor of the first stage.

3. $\frac{1}{2}$ - 1 Bit Switch

The $\frac{1}{2}$ - 1 Bit Switch selects either 1 or $\frac{1}{2}$ bit displacement of the early and late signals from the punctual signal. It also provides the driving circuitry for the channel mixers and outputs a punctual signal for purposes of oscilloscope display. Figures 35 and 36 give component layout and circuitry for this switch; Figure 37 shows an interface diagram. This unit requires +5 volts supply voltage.

Early and late signal outputs are produced by two sets of flip-flops: one set is clocked by a clock signal which is in-phase with the processing PN Gen. clock; this set of flip-flops produces the 1 bit displacement signals. The $\frac{1}{2}$ bit displacement signals are obtained by the second set of flip-flops: these devices are clocked by the inverted in-phase clock. Switching is achieved by grounding the Clear terminals of the unused set of flip-flops. Mixer drivers consist of 74S140 Schottky line drivers which are both parallel and series matched to 50 Ohm coaxial cable.

The PUNCTUAL STOP switch on this unit stops the punctual signal output but does not affect the early and late outputs; the purpose of this switch is to facilitate classroom demonstration by allowing the DLTL to maintain tracking while punctual channel despreading is started or stopped.

4. Bandpass Filters

Channel bandpass filters are four pole monolithic crystal (AT cut) filters manufactured by Piezo technology, Orlando, Florida. Specifications for each filter are listed in Table 5. Spurs on these filters are approximately 30 dB down from center frequency response. Maximum power capacity of these devices is approximately 5 mw. These crystal filters are also matched to their respective channels and should not be interchanged.

TABLE 5

MODEL 1985 BANDPASS CRYSTAL (MONOLITHIC) FILTER SPECIFICATIONS

Serial Number	1	2	3
Center Frequency (Mhz)	30.11293	30.11138	30.11089
Passband Ripple (dB)	.1	.5	.6
Insertion Flat Loss (dB)	2.3	2.0	2.5
Characteristics at -6 dB:			
f_h (Mhz)	30.12716	30.12560	30.12460
f_l (Mhz)	30.09870	30.09717	30.097.8
Bandwidth (KHz)	28.46	28.43	27.42
Characteristics at -30 dB:			
f_h (Mhz)	30.13930	30.13733	30.13484
f_l (Mhz)	30.08581	30.08463	30.08585
Bandwidth (Khz)	53.49	52.7	48.99

5. Other Components

a. Diode Detectors

A schematic diagram of diode detector circuitry is given as Figure 38. The early and late channel detectors are matched and have a 0.1 ms time constant RC filtered output. The punctual channel detector has a time constant of 4.6 microseconds to accommodate a larger message bandwidth. All diodes are 1N21WE point contact diodes; power levels applied to these devices should not exceed 14 dBm to avoid characteristic degradation. Output voltage vs. input power characteristics are shown as Figure 16.

b. Mixers

RELCOM M6A double balanced mixers are utilized for punctual, early, and late channel correlation. A schematic diagram of mixer circuitry is shown as Figure 39. Fifty Ohm resistors are used to match the mixer to the driving transmission line. Approximately 10 ma of drive current through the mixer 'I' port in either direction provides for minimum attenuation and either 0 or 180 degrees of phase shift of the signal passing from the 'L' port to the 'R' port.

These devices are characterized by a 1 dB compression point of approximately 2 dBm; below this level insertion loss of 1 dB is typical. Maximum power dissipation of these units is 50 mw.

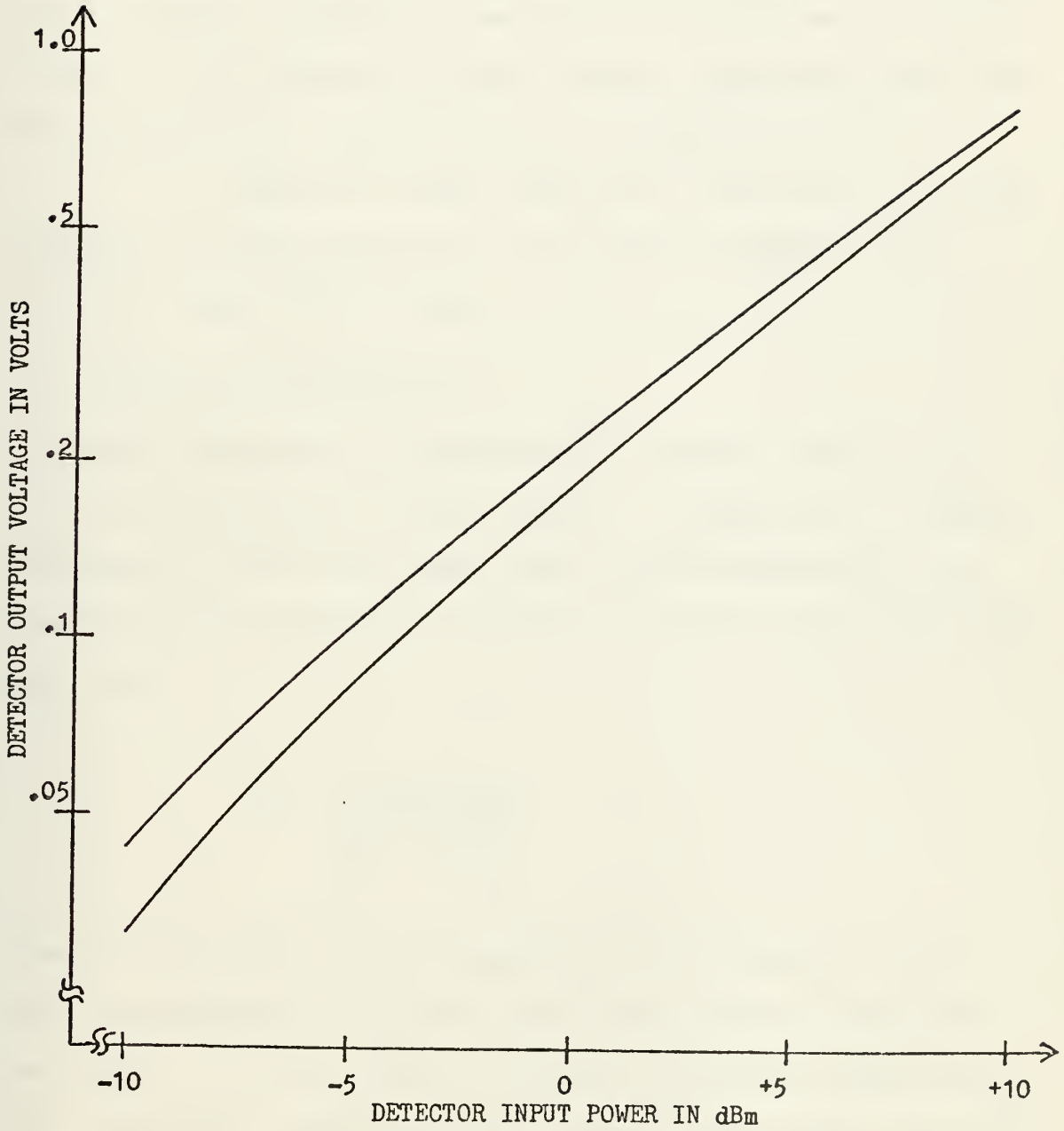


Figure 16. DETECTOR OUTPUT VOLTAGE AS A FUNCTION OF INPUT POWER

c. Combiners/Couplers

Three types of power distributing devices are utilized in the FSSS; all are compatible with 50 Ohm coaxial cable. Four way combiners (splitters) are used in receiving and processing subsystems and are characterized by approximately 6.5 dB insertion loss. Several power splitters are also used; their insertion loss is typically 3.5 dB.

Input to output insertion loss of the 11.5 dB couplers is approximately 1 dB; coupled output is 11.5 dB below input power level.

D. SYSTEM LOOP BANDWIDTH

Loop bandwidth calculations for a phase locked loop (PLL) are described in Reference A. Adaptation of these formulae to the first order DLTL is straightforward and results in the following formula for system loop bandwidth, B_L in Hz:

$$B_L = \frac{125\ (F)\ (G)}{\sqrt{1 + \frac{1}{S/N}}}$$

where F is either 1 or 2 depending upon whether 1 or $\frac{1}{2}$ bit displacement of the early and late channels has been selected. G is the gain of the loop difference amplifier, and S/N is the signal to noise ratio of the signal entering the IF Amplifier. These calculations are dependent upon the fact that the IF Amplifier is utilized in the AGC mode and that its power output is constant at 1 dBm.

IV. CONCLUSIONS

The design and utilization of a PN Generator/Correlator and a Flexible Spread Spectrum System in which it is employed has been presented.

The equipment is built and is functioning properly; no problems are presently known to exist in any part of the FSSS.

It is anticiapted that the FSSS will become a valuable educational aid to instruction, research and demonstration of spread spectrum techniques.

APPENDIX A

Appendix A contains Table 6 and Figures 17 thru 39. Table 6 is a listing of all integrated circuits used in the FSSS. Figures 17 thru 39 show layout, schematic and interface diagrams for the PN Generator/Correlator and other system components.

TABLE 6

INTEGRATED CIRCUITS USED IN THE FLEXIBLE SPREAD SPECTRUM SYSTEM

IC NUMBER	TYPE IC	DESCRIPTION
31	N7486	QUAD 2 Input EOR
32	N7404	HEX Inverter
33-36	5558	DUAL 741 OP AMP
101-103	N7400	QUAD 2 Input NAND
104, 105	N7404	HEX Inverter
111-113	N7418	TRIPLE 3 Input OR
121, 122	N7421	DUAL 4 Input AND
140, 141	74S140	DUAL 4 Input NAND Schottky Line Driver
171-177	N7476	DUAL J-K Flip-Flop
181-185	N7486	QUAD 2 Input EOR
191	9348	12 Input Parity Checker
201, 203	74S140	DUAL 4 Input NAND Schottky Line Driver
202	N7400	QUAD 2 Input NAND
204	N7486	QUAD 2 Input EOR
205	N7400	QUAD 2 Input NAND
206	N7476	DUAL J-K Flip-Flop
207-213	N7490	Divide-by-Ten Counter
402	N7402	QUAD 2 Input NOR
404	N7400	QUAD 2 Input NAND
441-444	74S140	DUAL 4 Input NAND Schottky Line Driver
471-473	N7476	DUAL J-K Flip-Flop

TABLE 6
(Continued)

IC NUMBER	TYPE IC	DESCRIPTION
481, 482	N7486	QUAD 2 Input EOR
601-604	N7404	HEX Inverter

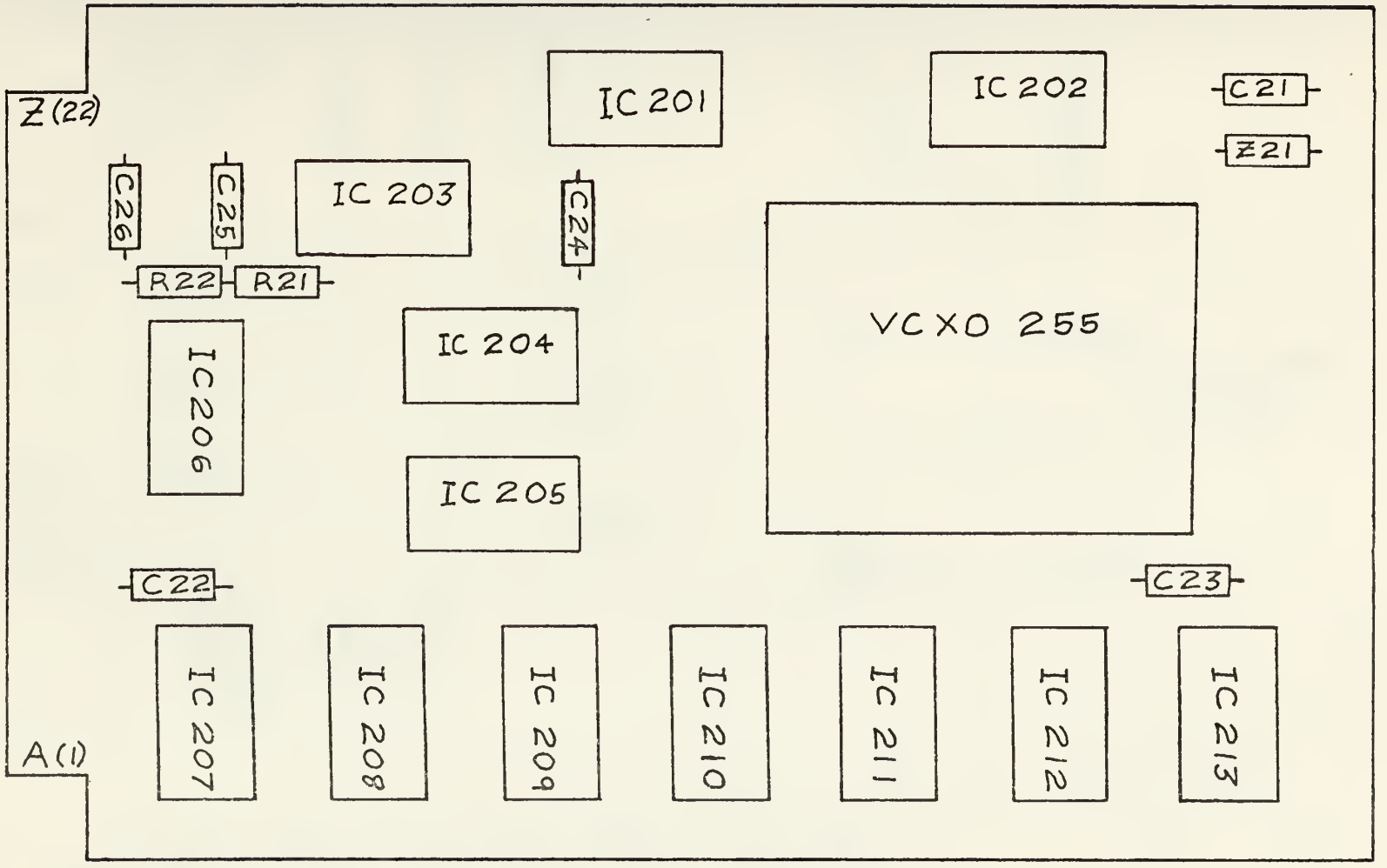


Figure 17. CLOCK (CLO) BOARD COMPONENT LAYOUT

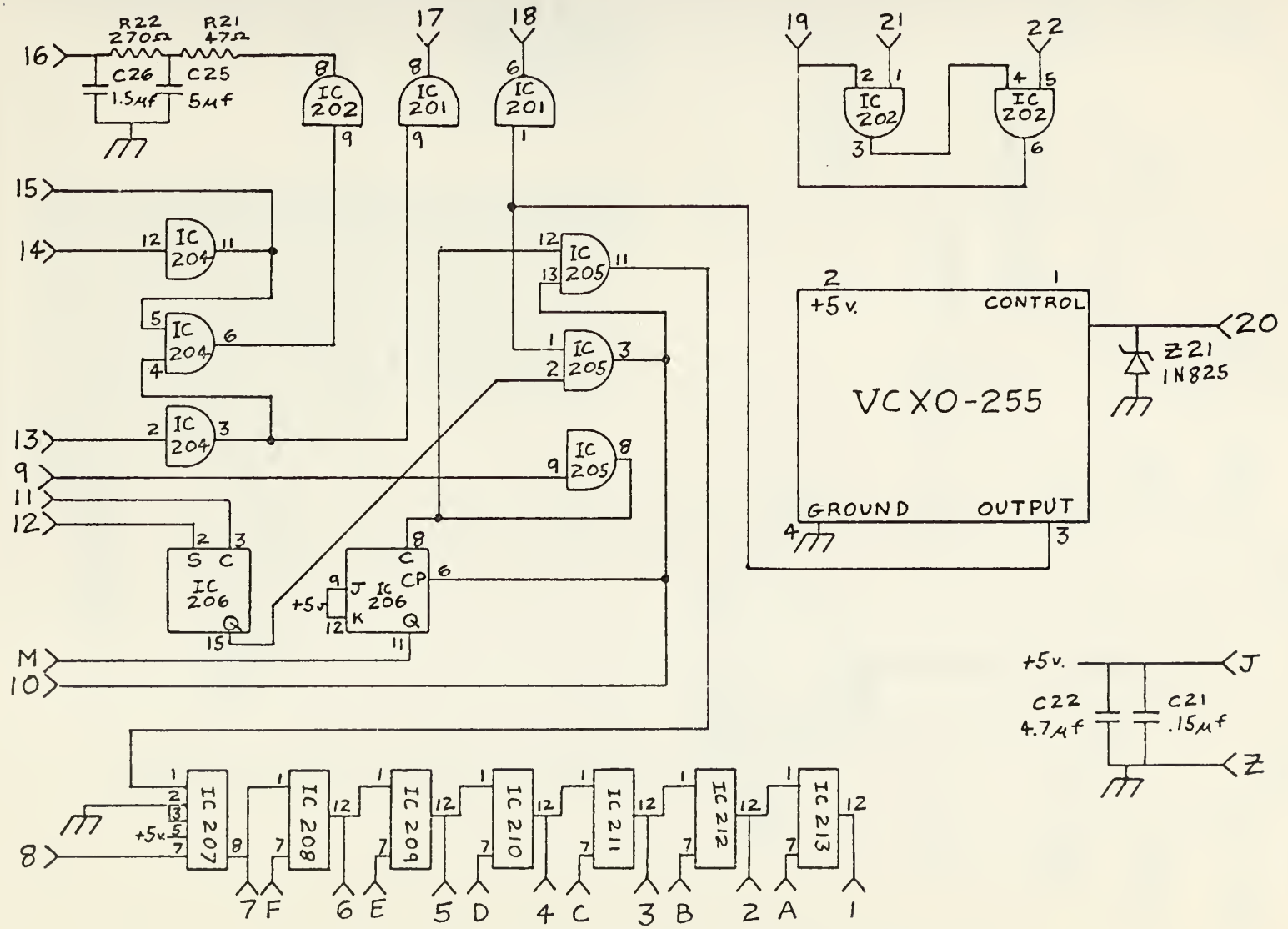


Figure 18. CLOCK BOARD SCHEMATIC DIAGRAM

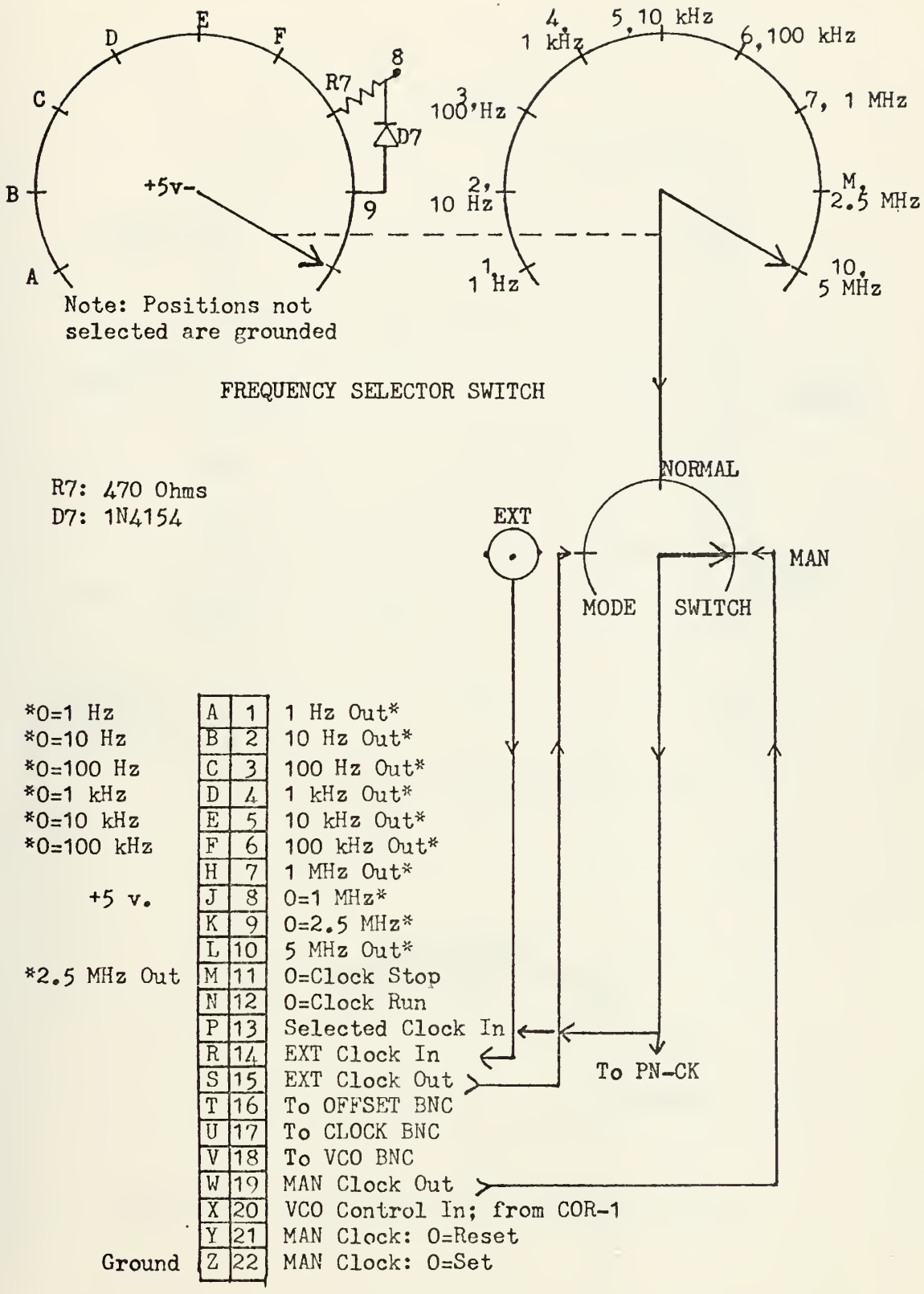
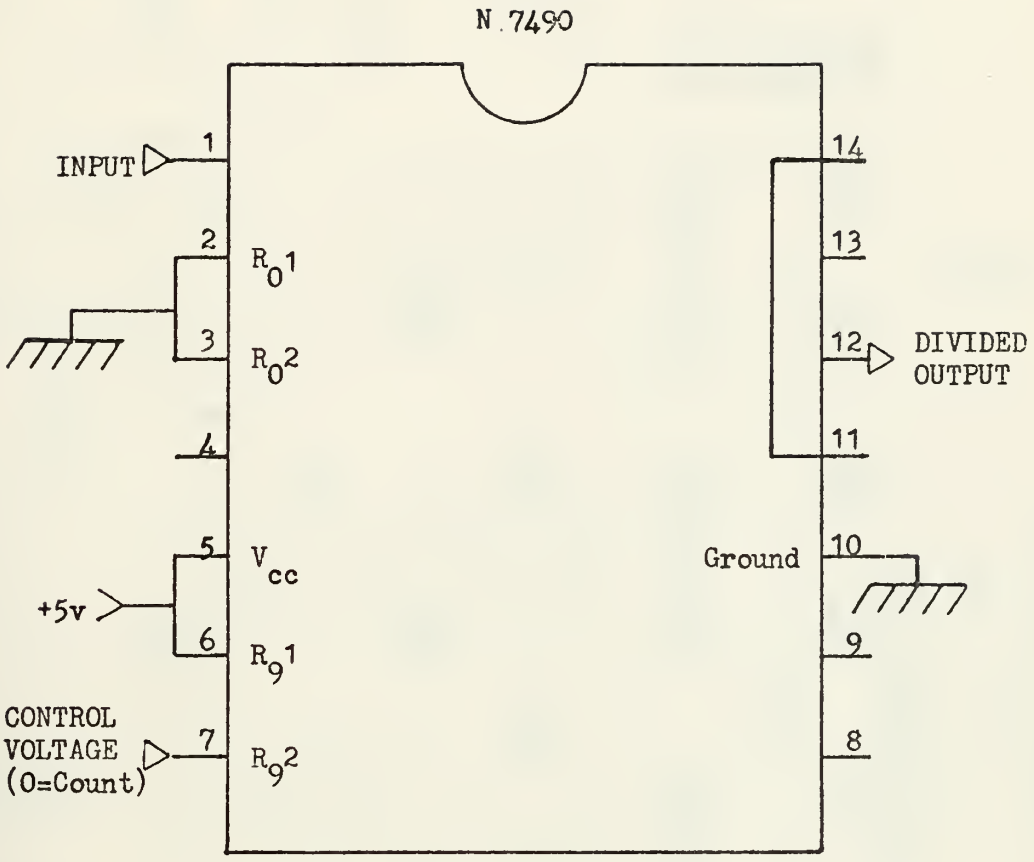


Figure 19. CLOCK BOARD INTERFACE DIAGRAM



TRUTH TABLE

$R_0$1	$R_0$2	$R_9$1	$R_9$2	
0	0	1	0	COUNT
0	0	1	1	INHIBIT

Figure 20. DIVIDE-BY-TEN COUNTER DETAIL

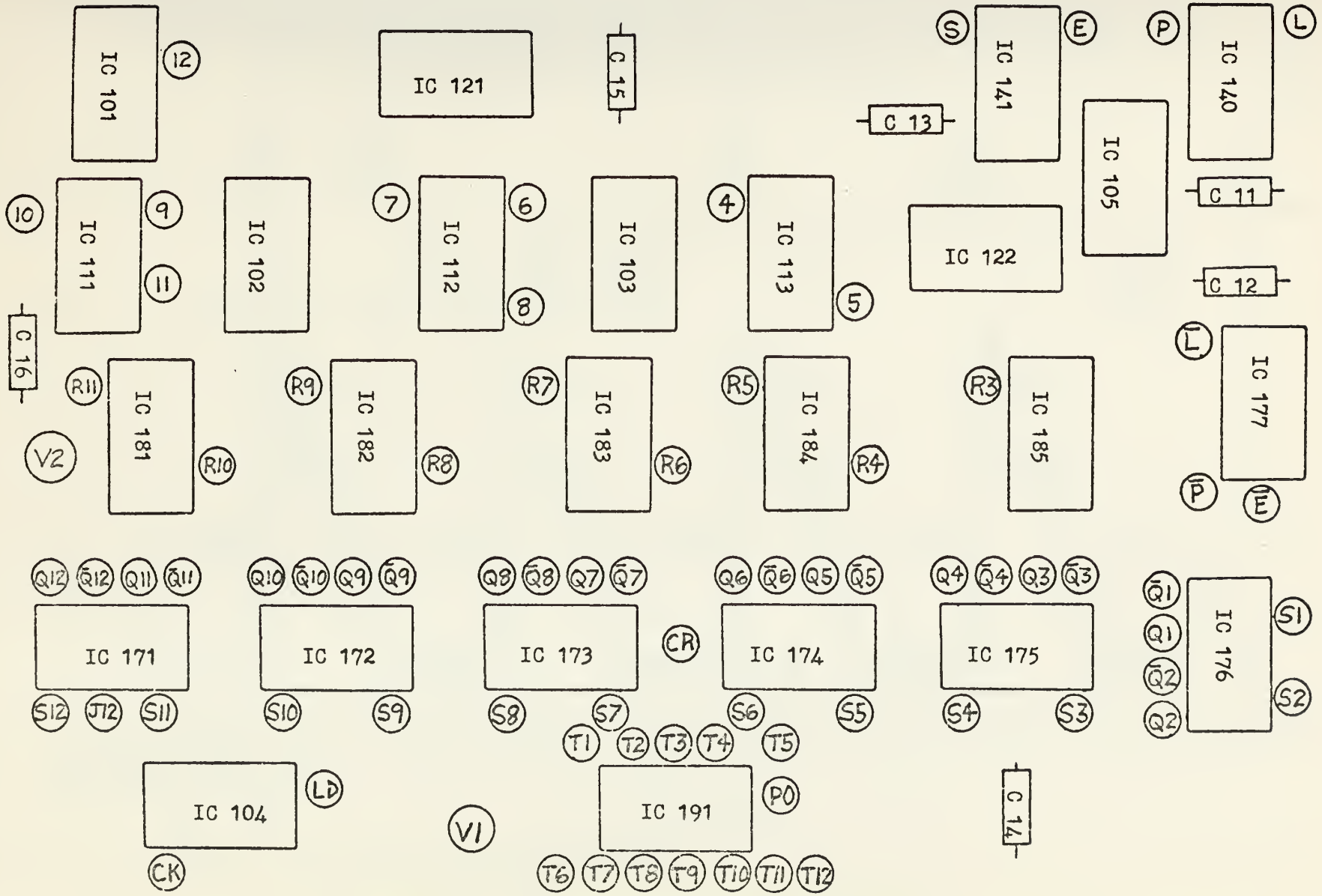


Figure 21. PN BOARD COMPONENT LAYOUT

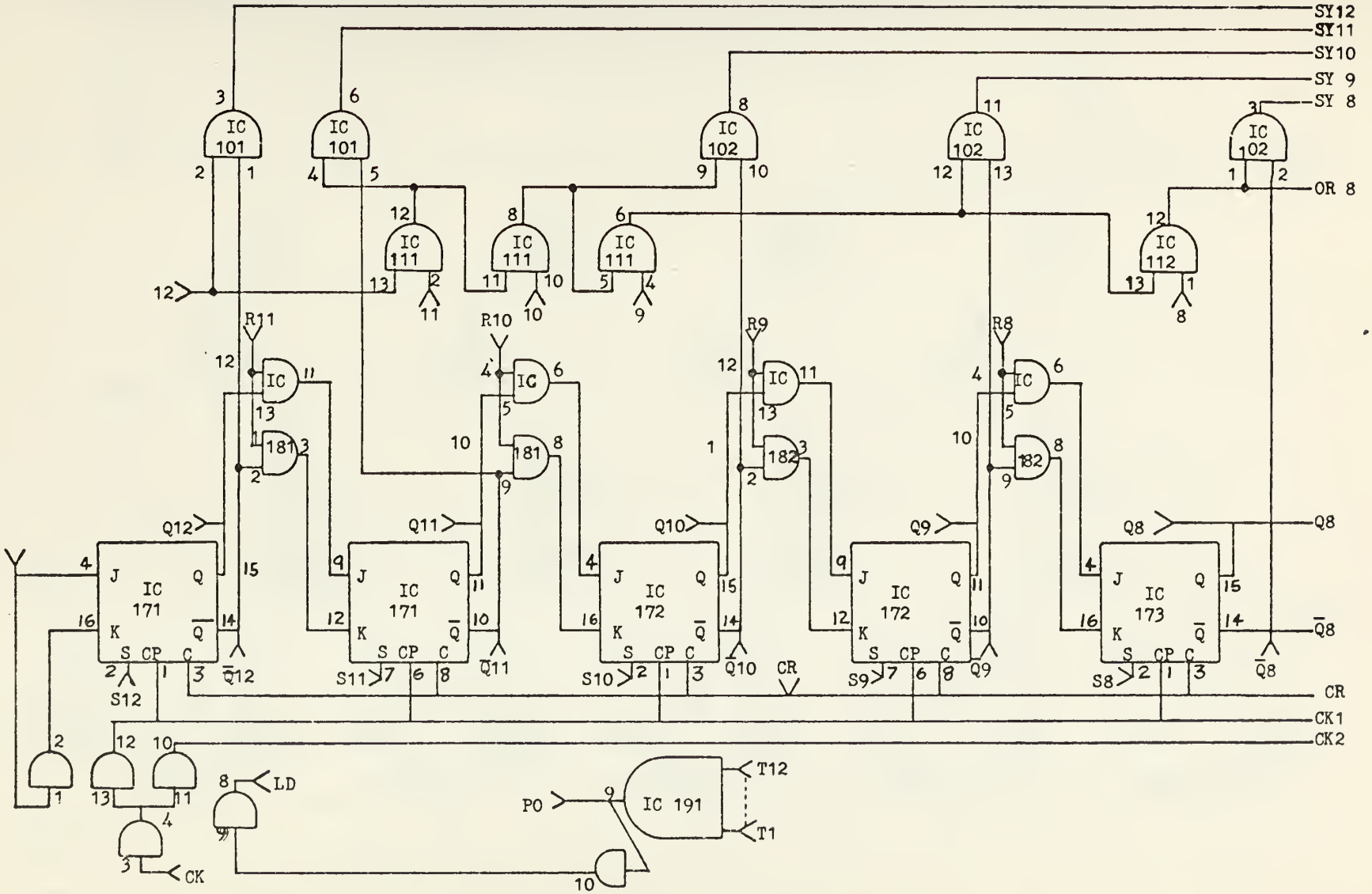


Figure 22. PN BOARD SCHEMATIC DIAGRAM

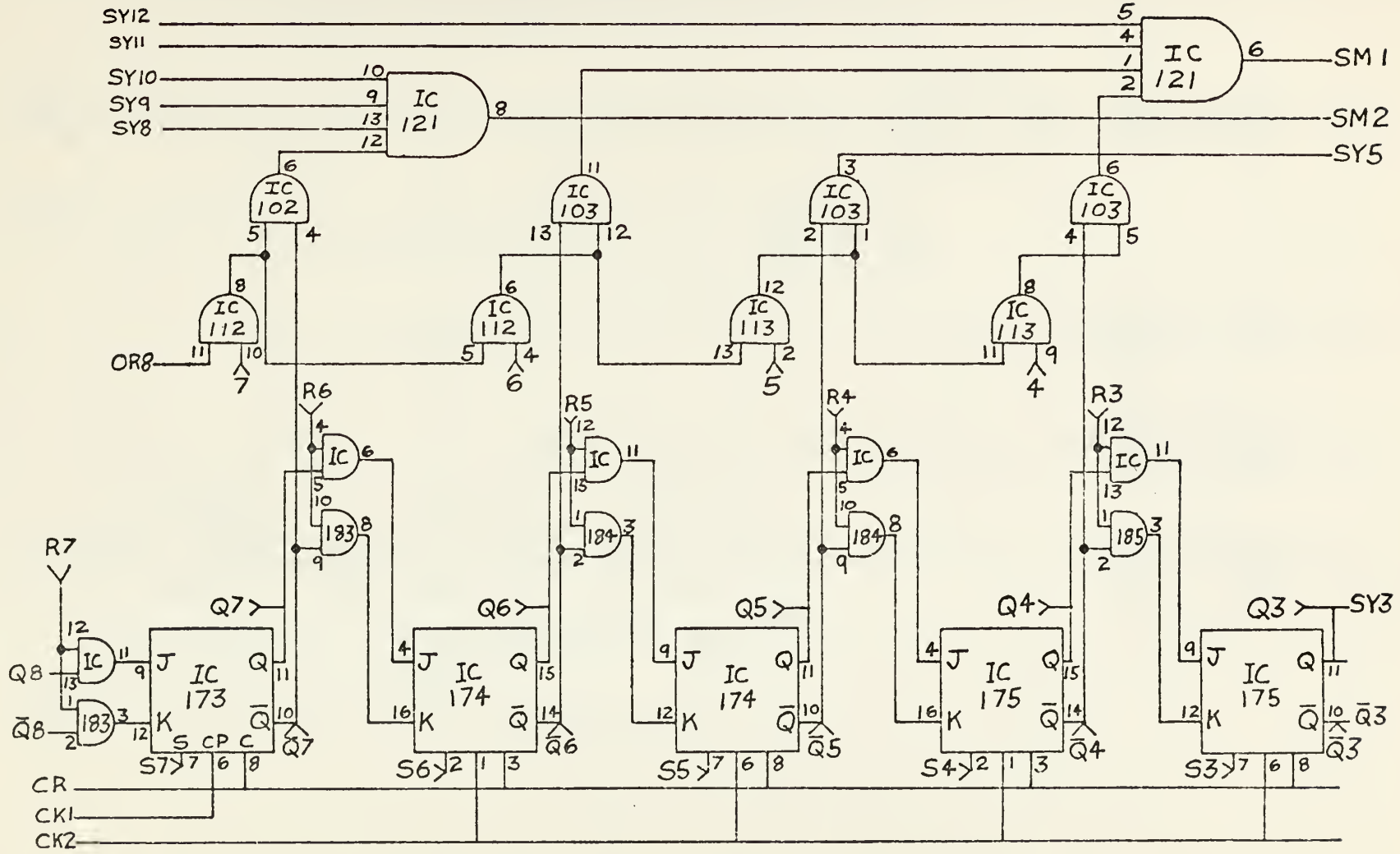


Figure 23. PN BOARD SCHEMATIC DIAGRAM

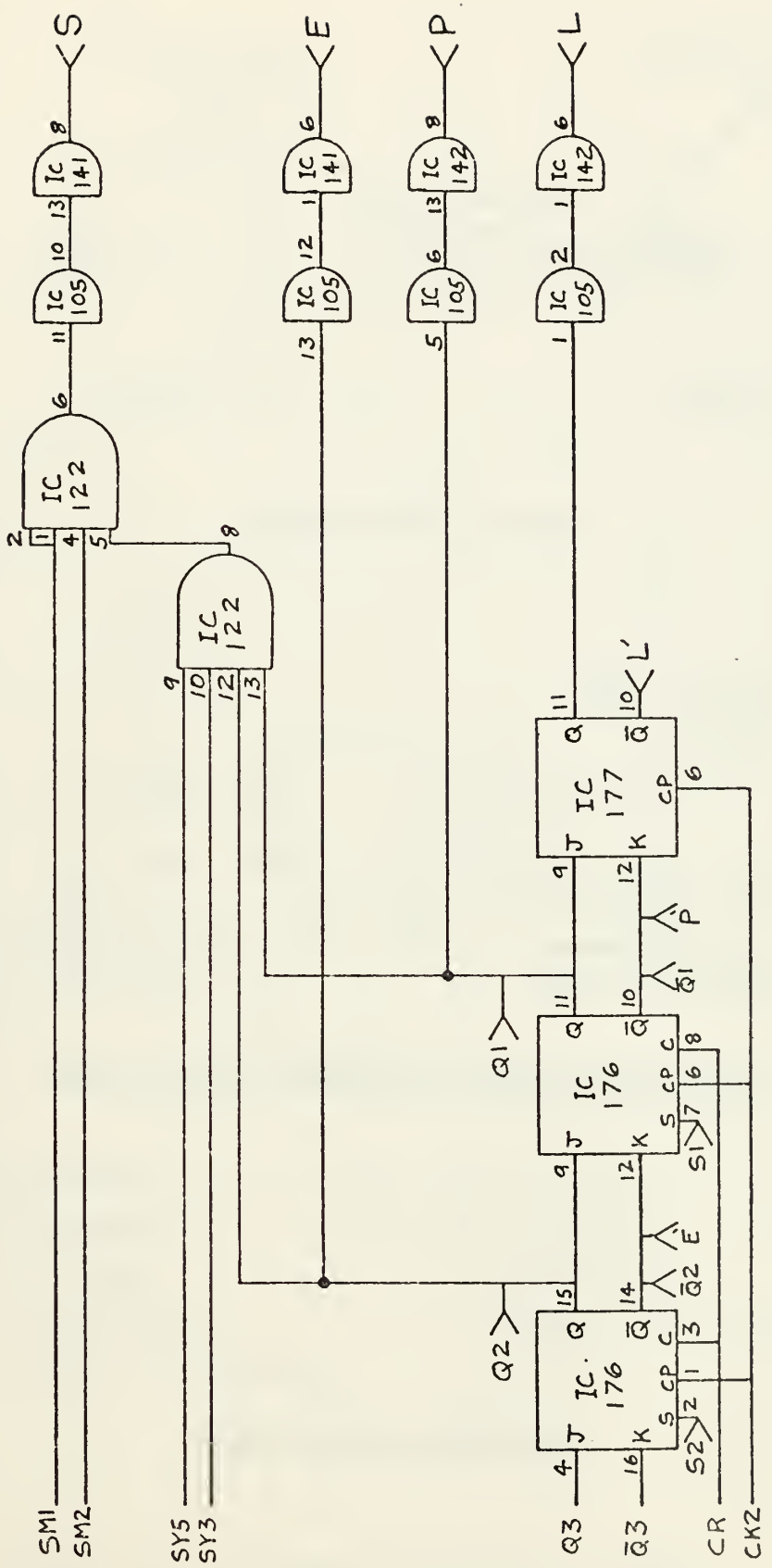
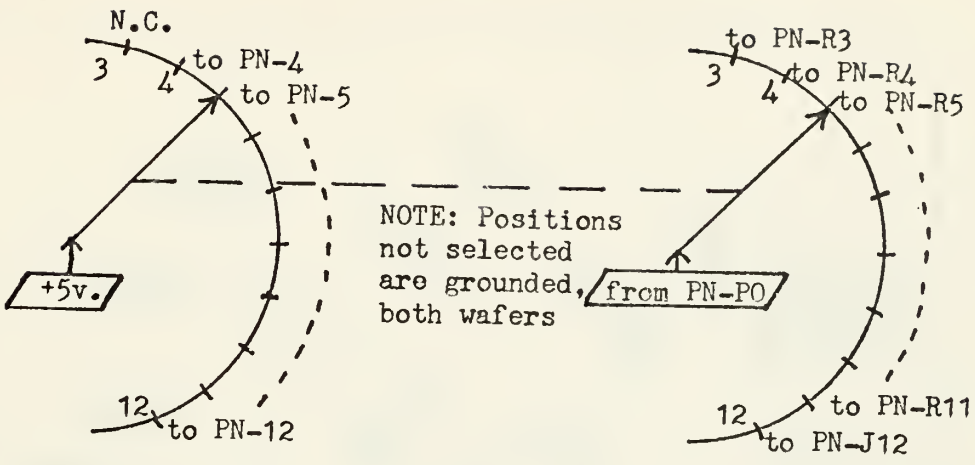
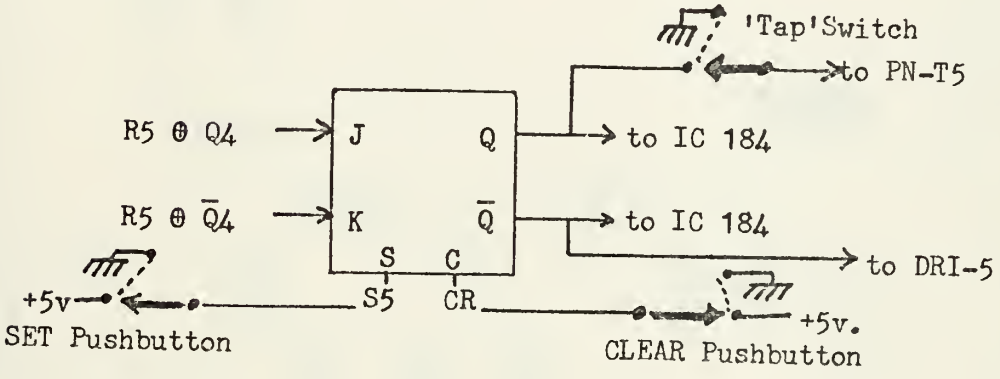


Figure 24. PN BOARD SCHEMATIC DIAGRAM



REGISTER LENGTH SWITCH



SAMPLE REGISTER CONNECTION DIAGRAM FOR POSITION 5

S - To SYNC BNC
E - To EARLY BNC
L - To LATE BNC
P - To PUNCTUAL BNC
LD- To MODULO TWO ADDER LED

$\overline{L}$ - To COR-20
$\overline{P}$ - To COR-21
$\overline{E}$ - To COR-22
CK- From CLO-13 (Clock)

OTHER EXTERNAL CONNECTIONS

Figure 25. PN BOARD INTERFACE DIAGRAM

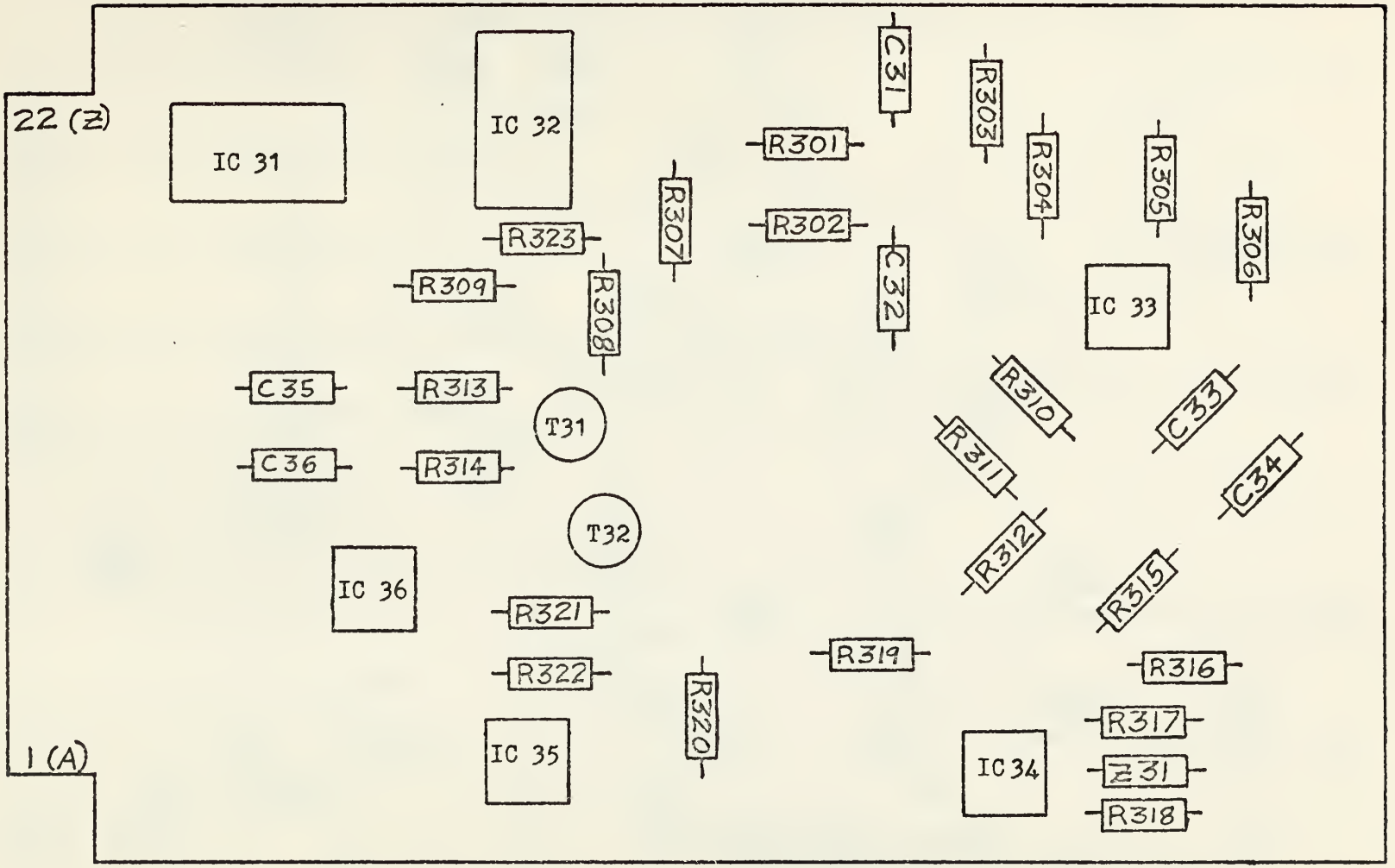


Figure 26. CORRELATOR BOARD (COR) COMPONENT LAYOUT

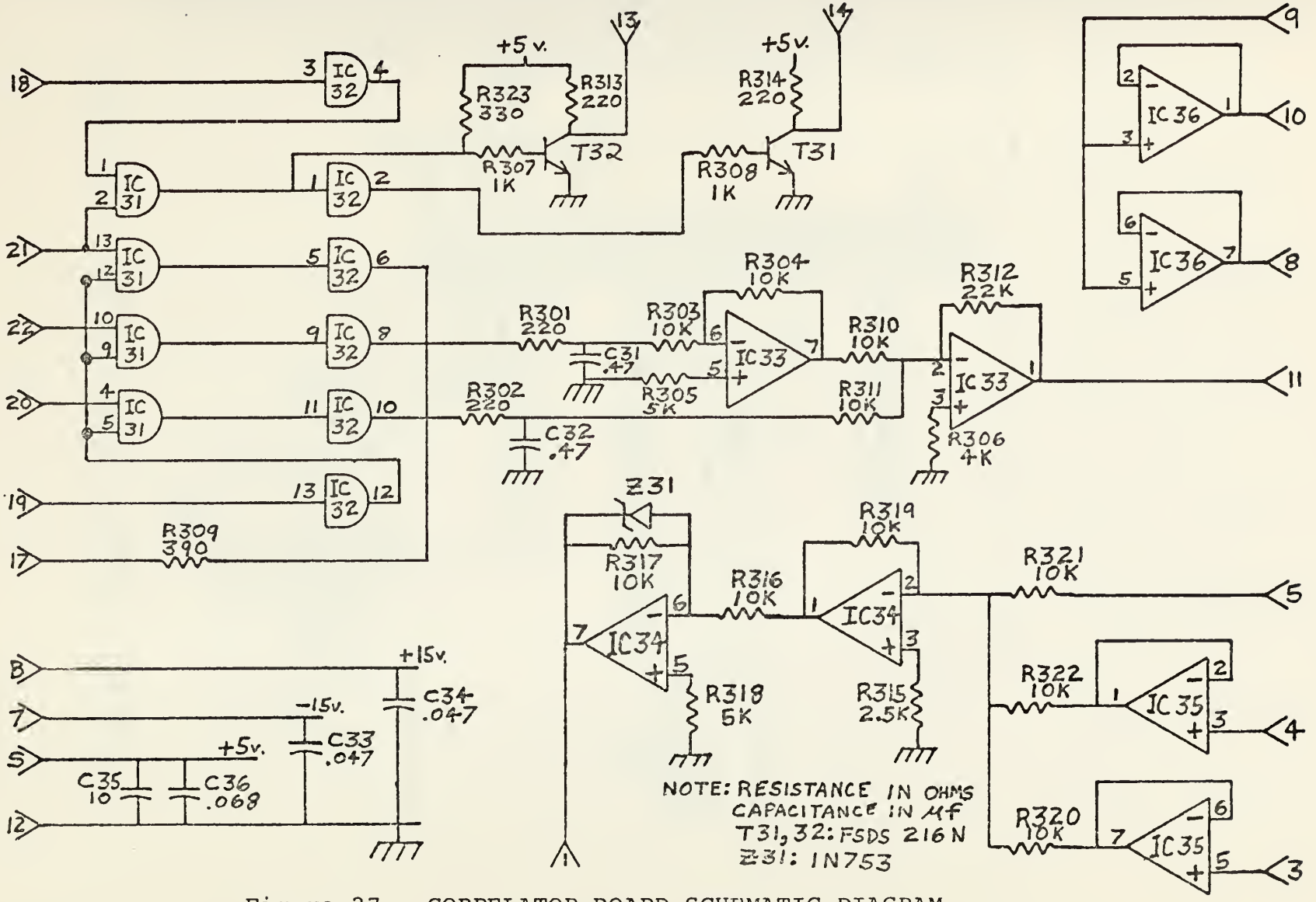


Figure 27. CORRELATOR BOARD SCHEMATIC DIAGRAM

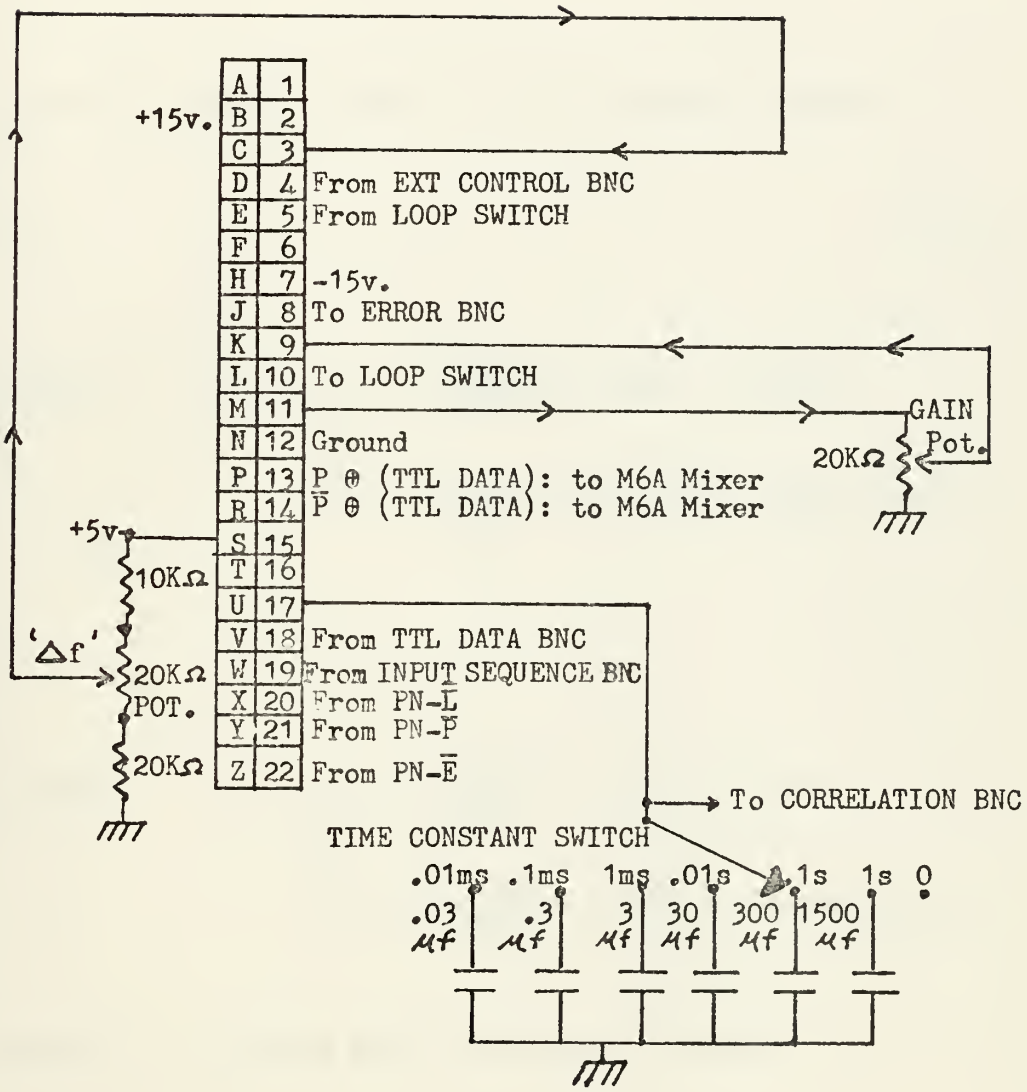


Figure 28. CORRELATOR BOARD INTERFACE DIAGRAM

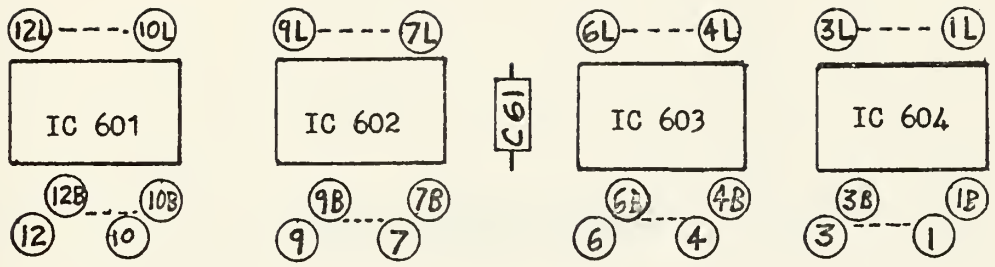


Figure 29. DRIVER BOARD (DRI) COMPONENT LAYOUT

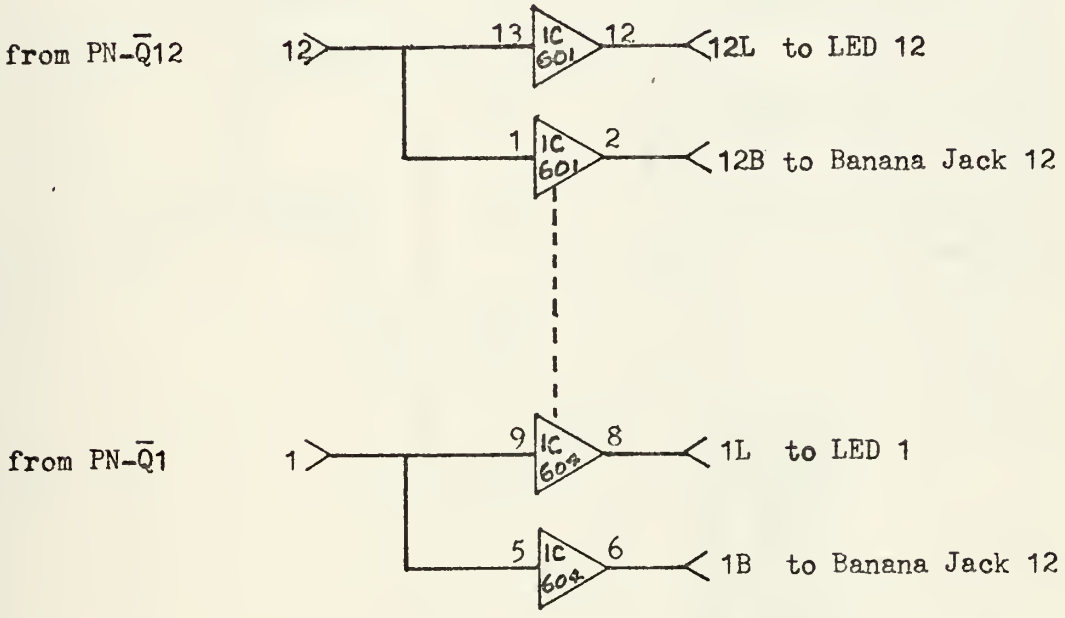


Figure 30. DRIVER BOARD SCHEMATIC DIAGRAM

PLUG TYPE: CANON DEM-9P

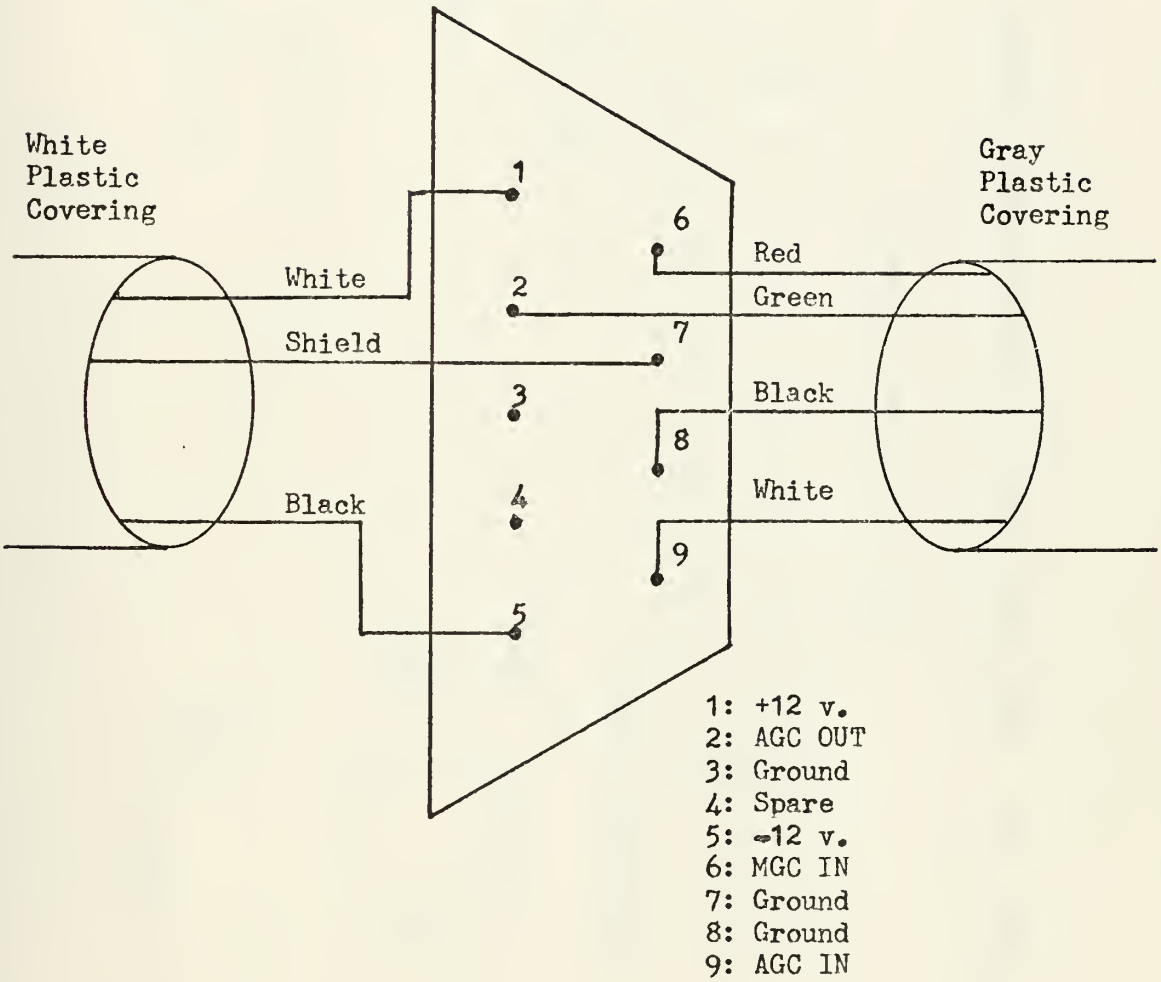


Figure 31. PIN CONNECTIONS FOR THE RHG IF AMPLIFIER

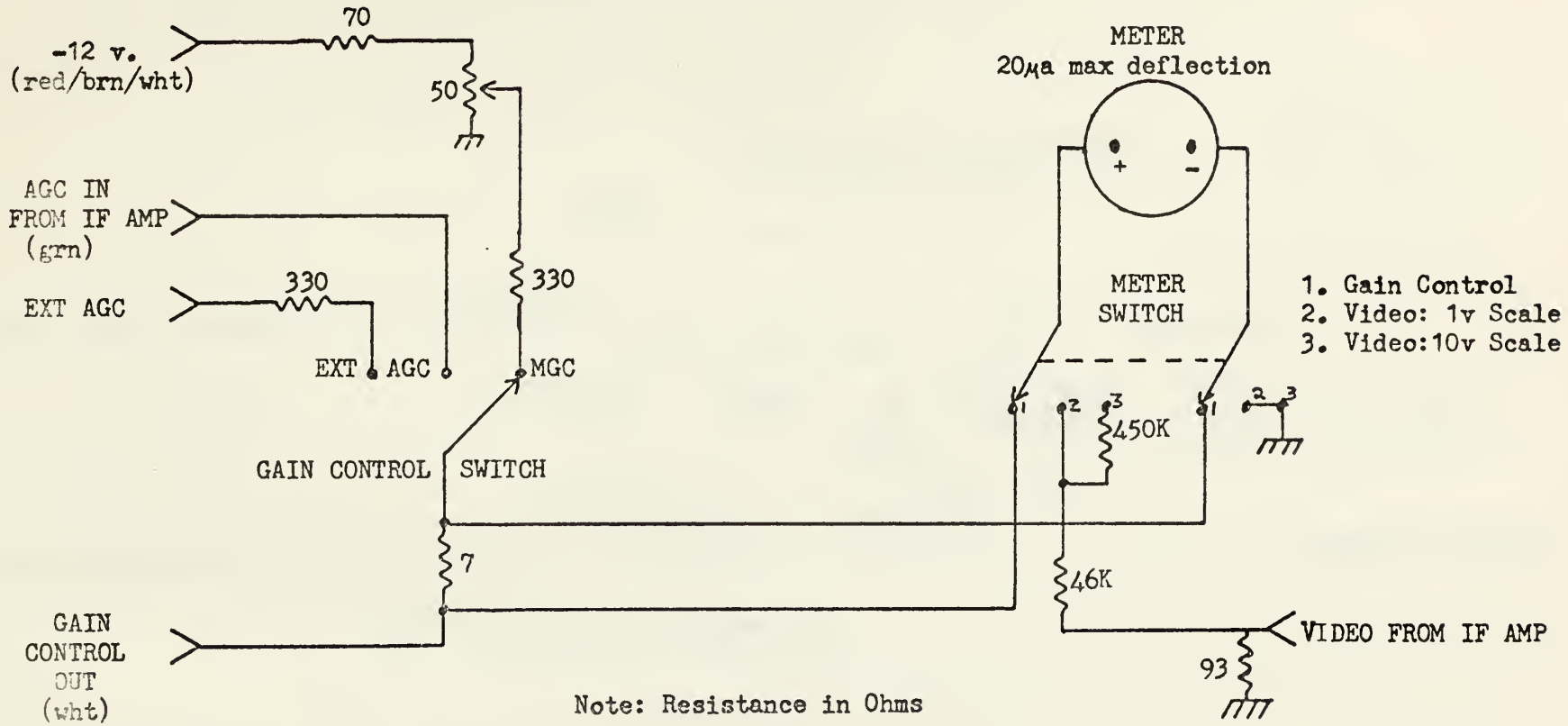
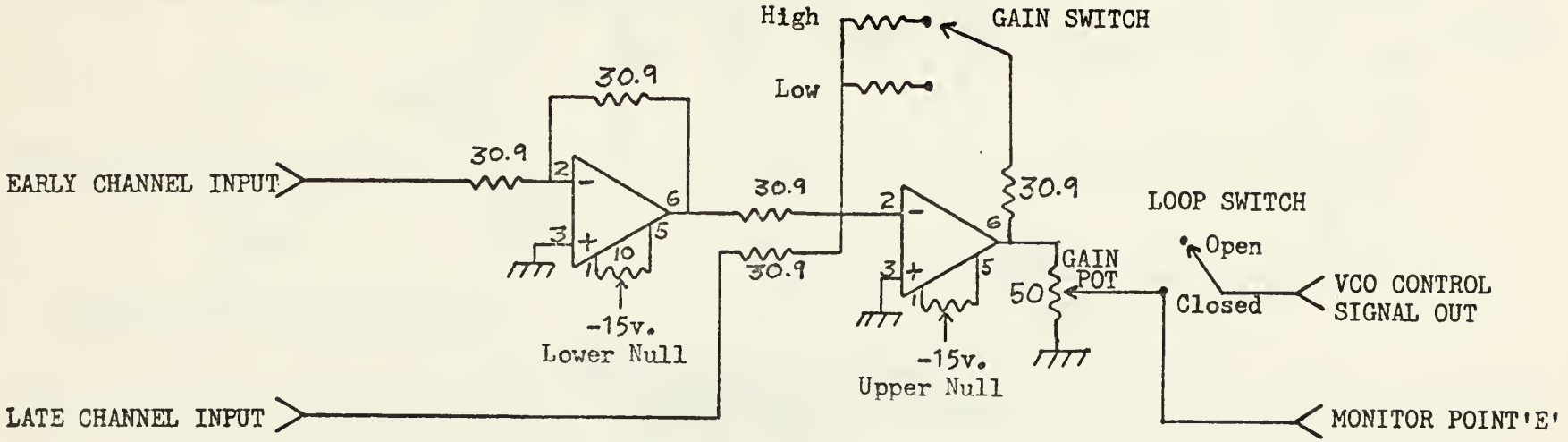
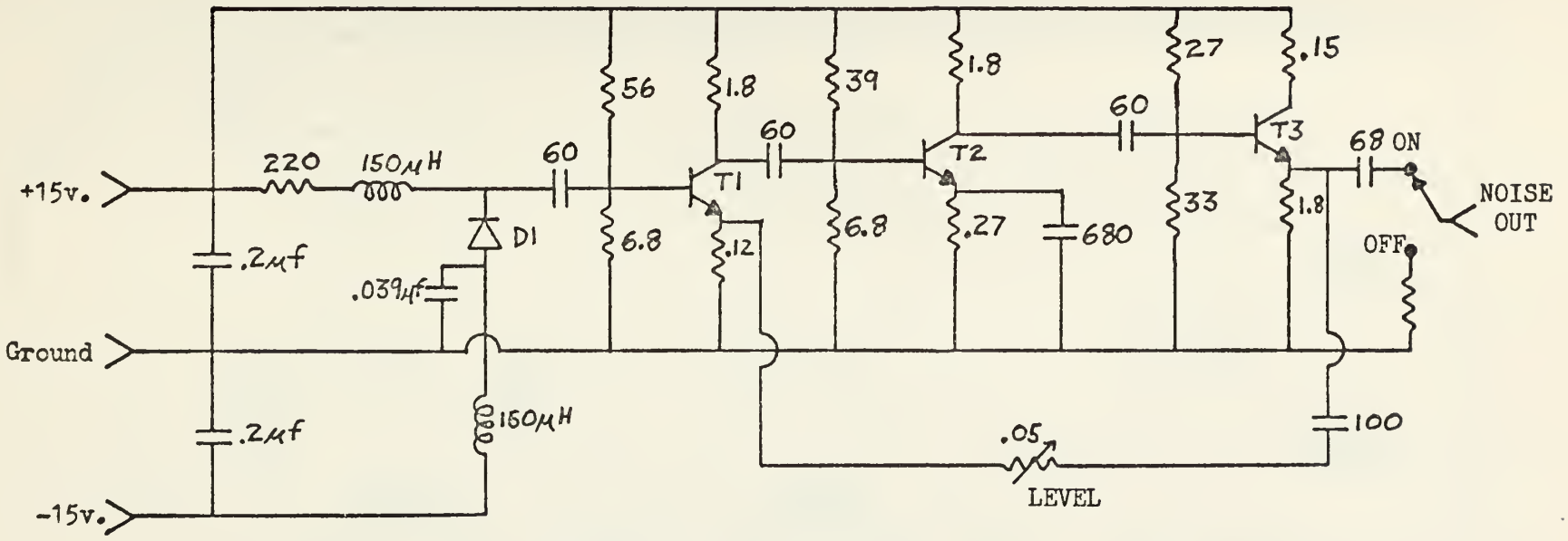


Figure 32. AMPLIFIER CONTROL/MONITOR UNIT SCHEMATIC DIAGRAM



NOTE: Resistance in K Ohms
OP AMPS: Burr Brown 3522K

Figure 33. DIFFERENCE AMPLIFIER/LOOP SWITCH SCHEMATIC DIAGRAM



NOTE: Resistance in K Ohms
Capacitance in Picofarads
T1-T3: 2N706A
D1: SR 1410-70

Figure 34. NOISE SOURCE SCHEMATIC DIAGRAM

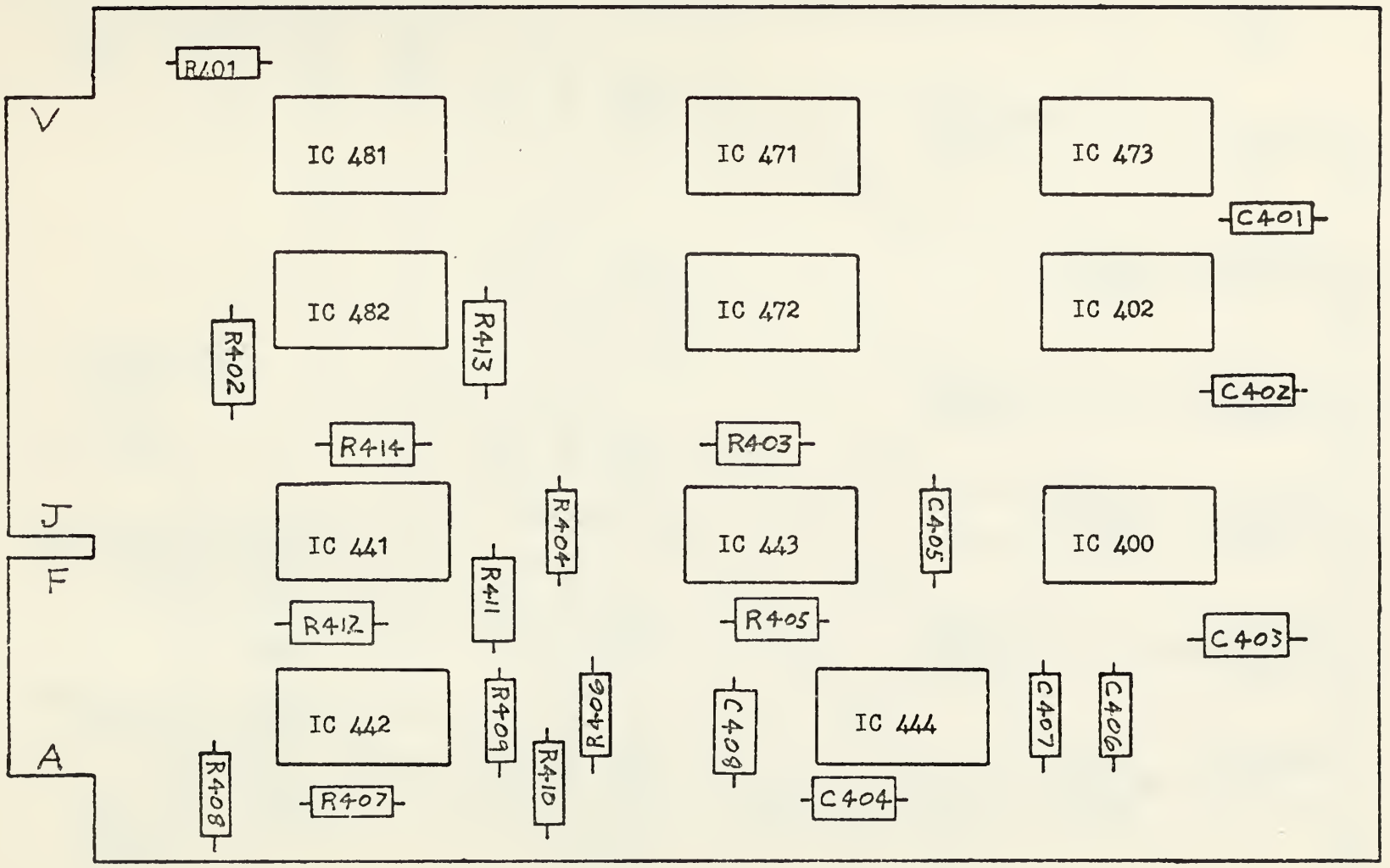


Figure 35. $\frac{1}{2}$ - 1 BIT SWITCH COMPONENT LAYOUT

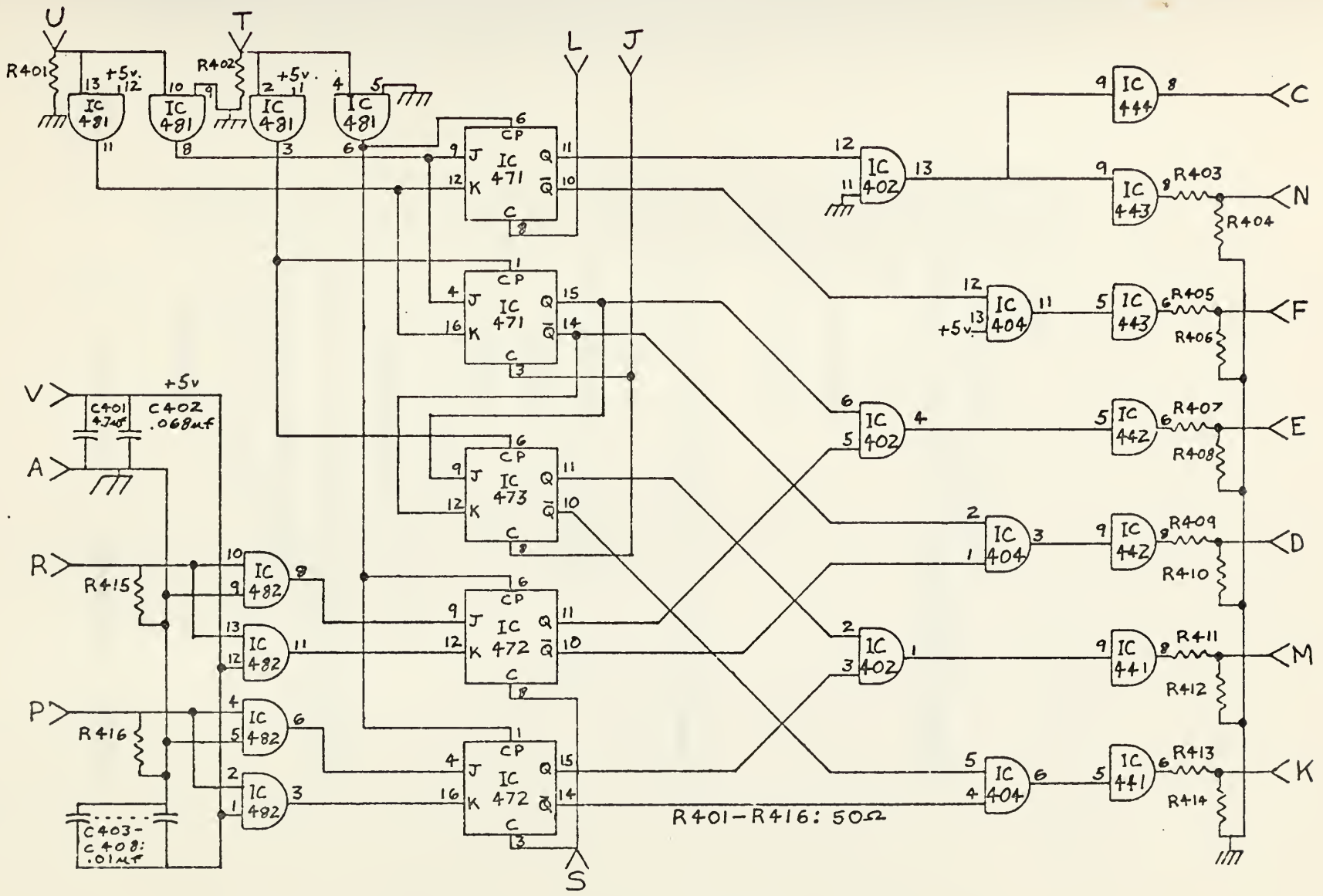


Figure 36. $\frac{1}{2}$ - 1 BIT SWITCH SCHEMATIC DIAGRAM

A	Ground
B	+5 Volts Out to Switches
C	PUNCTUAL Signal (For Oscilloscope Display)
D	$\overline{E}$ to Mixer
E	E to Mixer
F	$\overline{P}$ to Mixer
J	From $\frac{1}{2}$-1 Bit Switch:0= 1 Bit Displacement
K	$\overline{L}$ to Mixer
L	From PUNCTUAL STOP Switch: 0= Stop
M	L to Mixer
N	P to Mixer
P	L Input from PN Gen.
R	E Input from PN Gen.
S	From $\frac{1}{2}$-1 Bit Switch:0= $\frac{1}{2}$ Bit Displacement
T	Clock Input from PN Gen.
U	P Input from PN Gen.
V	+5 Volts Input

Figure 37. $\frac{1}{2}$ - 1 BIT SWITCH INTERFACE DIAGRAM

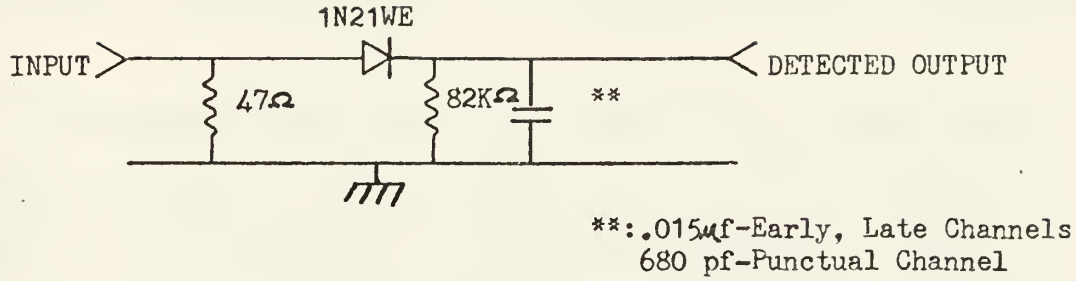


Figure 38. DIODE DETECTOR SCHEMATIC DIAGRAM

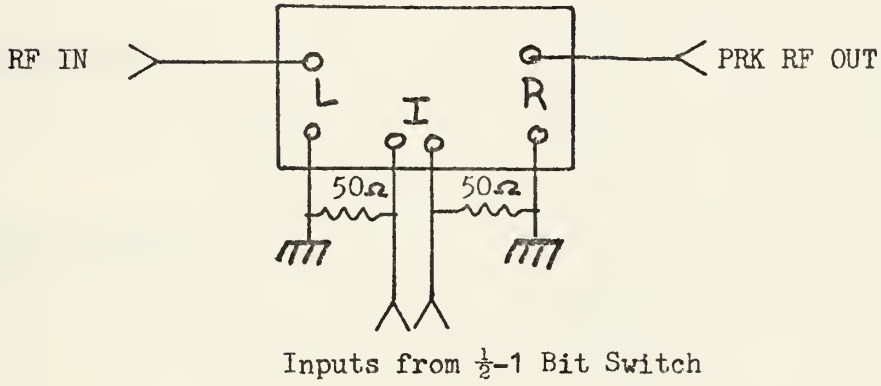


Figure 39. RELCOM M6A MIXER SCHEMATIC DIAGRAM

APPENDIX B

PN SEQUENCE GENERATING CODES FOR REGISTER LENGTHS 3 THROUGH 12

To generate a PN Sequence by a particular length shift register, switch the TAP switches listed in a particular column to the IN position. Reference to Figure 4. will assist in switch identification. Register position 1 is always tapped and is not listed for convenience.

REGISTER LENGTH 3

2	3

REGISTER LENGTH 4

2	4

REGISTER LENGTH 5

3	4	3 4 5	2 3 4
2 3 5	2 4 5		

REGISTER LENGTH 6

2	6	2 3 6	2 5 6
3 4 6	2 4 5		

REGISTER LENGTH 7

4	5	2 3 4	5 6 7
3 4 5	4 5 6	2 3 5 6 7	2 3 4 6 7
2 3 4 5 6	3 4 5 6 7	3 5 7	2 4 6
2	7	2 4 7	2 5 7
3 6 7	2 3 6		

REGISTER LENGTH 8

3 4 5	5 6 7	4 6 7	3 4 6
2 3 6 7 8	2 3 4 7 8	2 4 6	4 6 8
3 6 7	3 4 7	2 6 7	3 4 8
2 3 4 5 7	3 5 6 7 8	2 7 8	2 3 8

REGISTER LENGTH 9

4 6 7 8 9	2 3 4 5 7	2 6 7 8 9	2 3 4 5 9
5	6	4 5 7	4 6 7
5 6 9	2 5 6	2 5 9	2 6 9
3 4 6	5 7 8	2 3 5 6 7	4 5 6 8 9
6 7 9	2 4 5	2 4 5 7 8	3 4 6 7 9
3 8 9	2 3 8	3 4 7 8 9	2 3 4 7 8
2 5 6 7 9	2 4 5 6 9	2 4 7 8 9	2 3 4 7 9
3 4 5 6 7	4 5 6 7 8	3 5 7 8 9	2 3 4 6 8
3 5 8	3 6 8	3 4 5 6 8	3 5 6 7 8
2 4 5 6 7 8 9	2 3 4 5 6 7 9	3 5 9	2 6 8
2 3 5 6 8	3 5 6 8 9	2 3 4 8 9	2 3 7 8 9
2 4 6 7 9	2 4 5 7 9	2 3 4 6 7	4 5 7 8 9

REGISTER LENGTH 10

4	8	3 4 9	3 8 9
4 5 6 7 8 9 10	2 3 4 5 6 7 8	2 3 4 6 7	5 6 8 9 10
3 4 7 9 10	2 3 5 8 9	2 4 5 6 7 8 9	3 4 5 6 7 8 10
2 4 5	7 8 10	2 6 9	3 6 10
5 6 9	3 6 7	2 5 10	2 7 10
2 6 7 9 10	2 3 5 6 10	3 6 7 8 9	3 4 5 6 9
4 5 9	3 7 8	2 3 4 5 6 7 10	2 5 6 7 8 9 10
3 5 7 9 10	2 3 5 7 9	2 3 4 8 9	3 4 8 9 10
4 5 6 9 10	2 3 6 7 8	2 5 7 8 10	2 4 5 7 10
2 3 7 9 10	2 3 5 9 10	2 5 8 9 10	2 3 4 7 10
2 3 7 8 9	3 4 5 9 10	2 3 5 7 8	4 5 7 9 10
3 5 6 8 10	2 4 6 7 9	3 4 6	6 8 9
3 4 5 6 7 9 10	2 3 5 6 7 8 9	4 5 6 7 10	2 5 6 7 8
2 3 6	6 9 10	3 5 10	2 7 9
2 3 4 5 7 8 10	2 4 5 7 8 9 10	4 8 10	2 4 8

REGISTER LENGTH 11

2 4 9 10 11
2 4 5 6 7 10 11
2 3 5 8 11
2 3 7 10 11
3 6 7 8 9 10 11
2 4 11
2 3 6 9 11
2 6 7
2 3 4 5 7 8 10
6 7 8
6 10 11
5 8 9 10 11
4 9 10
2 5 7 8 9 10 11
3 6 9
2 4 5 8 11
5 8 10
3 4 5 8 10
4 6 8
5 6 7 10 11
3 6 7 9 10
5 6 9 10 11
2 4 6
5 6 7 8 10
4 5 9 10 11
3 4 5 6 8 9 10
4 5 7 8 9
3 5 6 7 9 10 11
2 3 10
3 4 6
2 3 4 5 8 10 11
4 8 11
3 4 6 9 11

2 3 4 9 11
2 3 6 7 8 9 11
2 5 8 10 11
2 3 6 10 11
2 3 4 5 6 7 10
2 9 11
2 4 7 10 11
6 7 11
3 5 6 8 9 10 11
5 6 7
2 3 7
2 3 4 5 8
3 4 9
2 3 4 5 6 8 11
4 7 10
2 5 8 9 11
3 5 8
3 5 8 9 10
5 7 9
2 3 6 7 8
3 4 6 7 10
2 3 4 7 8
7 9 11
2 4 5 6 7
2 3 4 8 9
3 4 5 7 8 9 10
4 5 6 8 9
2 3 4 6 7 8 10
3 10 11
7 9 10
2 3 5 8 9 10 11
2 5 9
2 4 7 9 10

3 7 9
2 4 5 7 9
3 5 6 8 10
2 6 8 10 11
2 4 6 8 9
2 4 5 6 8 10 11
3
2 3 4 5 6 7 9
4 7 8 9 10
2 5 6 8 11
2 5 6 9 10
2 3 4 7 8 10 11
2 3 6 8 9 10 11
6 7 10
2 5 6 7 9
2 5 6 8 10
4 7 8 9 11
2 3 5 6 7 8 9
3 4 6 7 8 9 10
3 8 10
2 3 7 9 11
3 4 8
2 4 5 6 8 9 11
2 3 7 8 11
2 3 8 9 10
3 4 5 6 8 9 11
3 5 6 7 9
2 3 4 5 11
2 4 6 8 10
2 5 10
4 5 6 7 10
3 4 7 8 9 10 11
2 8 9

4 6 10
4 6 8 9 11
3 5 7 8 10
2 3 5 7 11
4 5 7 9 11
2 3 5 7 8 9 11
10
4 6 7 8 9 10 11
3 4 5 6 9
2 5 7 8 11
3 4 7 8 11
2 3 5 6 9 10 11
2 3 4 5 7 10 11
3 6 7
4 6 7 8 11
3 5 7 8 11
2 4 5 6 9
4 5 6 7 8 10 11
3 4 5 6 7 9 10
3 5 10
2 4 6 10 11
5 9 10
2 4 5 7 8 9 11
2 5 6 10 11
3 4 5 10 11
2 4 5 7 8 9 10
4 6 7 8 10
2 8 9 10 11
3 5 7 9 11
3 8 11
3 6 7 8 9
2 3 4 5 6 9 10
4 5 11

REGISTER LENGTH 11 (Continued)

2 4 5 6 7	6 7 8 9 11	3 4 6 8 9 10 11	2 3 4 5 7 9 10
4 6 9	4 7 9	3 5 6 7 8 9 11	2 4 5 6 7 8 10
2 6 7 9 11	2 4 6 7 11	2 5 6 7 8 10 11	2 3 5 6 7 8 11
3 4 6 7 9 10 11	2 3 4 6 7 9 10	3 4 11	2 9 10
2 5 8 9 10	3 4 5 8 11	3 4 5 7 8 10 11	2 3 5 6 8 9 10
2 3 4 5 8 9 11	2 4 5 8 9 10 11	2 3 6 7 8 9 10	3 4 5 6 7 10 11
2 6 7 8 11	2 5 6 7 11	2 3 6 8 10	3 5 7 10 11
5 6 7 9 11	2 4 6 7 8	2 3 6 7 9	4 5 6 10 11
4 5 7 9 10	3 4 6 8 9	2 3 4 6 7 9 11	2 4 6 7 9 10 11
3 4 5 7 9 10 11	2 3 4 6 8 9 10	2 4 8 9 10	3 4 5 9 11
8 10 11	2 3 5	5 6 8	5 7 8

REGISTER LENGTH 12

2 3 6 8 9 10 12	2 4 5 6 8 11 12	3 4 10	4 10 11
5 8 9 10 12	2 4 5 6 9	2 3 4 9 10	4 5 10 11 12
4 5 6 9 10	4 5 8 9 10	3 4 6 8 11	3 6 8 10 11
3 4 5 7 12	2 7 9 10 11	2 3 5 6 11	3 8 9 11 12
2 3 4 7 8 9 12	2 5 6 7 10 11 12	2 5 7	7 9 12
3 5 6 7 9 10 11	3 4 5 7 8 9 11	3 7 9 10 11	3 4 5 6 8 9 10 11 12
2 4 5 6 8 9 10 11 12	3 4 5 7 11	2 3 4 5 8 11 12	2 3 6 9 10 11 12
5 7 10 11 12	2 3 4 7 9	4 7 8 9 12	2 5 6 7 10
5 7 9 11 12	2 3 5 7 9	2 4 5 7 9 11 12	2 3 5 7 9 10 12
2 3 5 7 12	2 7 9 11 12	6 7 8 10 12	2 4 6 7 8
5 7 8 10 12	2 4 6 7 9	4 5 6 8 10	4 6 8 9 10
2 3 5 8 12	2 6 9 11 12	4 5 7 10 11	3 4 7 9 10
3 4 5 6 8 9 12	2 5 6 8 9 10 11	2 3 6 11 12	2 3 8 11 12
2 3 4 8 10 11 12	2 3 4 5 6 8 9 10 12	2 4 6 10 12	2 4 8 10 12
3 4 5 6 8 10 11	3 4 6 8 9 10 11	3 4 7 9 11	3 5 7 10 11
2 3 4 7 11	3 7 10 11 12	2 5 6 8 9	5 6 8 9 12
2 3 4 5 9 10 12	2 4 5 9 10 11 12	2 3 6 7 11	3 7 8 11 12
3 4 7 11 12	2 3 7 10 11	2 3 4 6 10 11 12	2 3 4 5 6 8 9 10 11
3 7 8 9 11	3 5 6 7 11	2 3 9 11 12	2 3 5 11 12
4 7 8 9 10 11 12	2 3 4 5 6 7 10	7 8 9 10 12	2 4 5 6 7

REGISTER LENGTH 12 (Continued)

4 6 7
2 3 5 6 10
2 3 4 6 7 8 12
2 3 4 5 9
5 7 8
2 4 6 7 8 9 11
2 5 7 8 9 10 12
2 3 6 7 10 11 12
4 5 9 10 11
2 3 5 7 8 9 11
2 5 8 9 11
3 8 9
5 8 12
2 3 11
2 4 7 8 10
2 3 4 5 6 9 10

7 8 10
4 8 9 11 12
2 6 7 8 10 11 12
5 9 10 11 12
6 7 9
3 5 6 7 8 10 12
2 4 5 6 7 9 12
2 3 4 7 8 11 12
3 4 5 9 10
3 5 6 7 9 11 12
3 5 6 9 12
5 6 11
2 6 9
3 11 12
4 6 7 10 12
4 5 8 9 10 11 12

6 9 10
3 5 10 11 12
7 8 9 10 11
2 4 9 10 12
2 4 5 9 12
3 5 9 10 11
3 6 7 9 12
2 3 6 8 11
5 6 7 9 10
4 5 6 8 12
4 7 8 11 12
2 4 8 9 12
3 4 5 6 10
2 3 4 5 7 8 9
5 11 12
2 5 6 7 8 11 12

4 5 8
2 3 4 9 11
3 4 5 6 7
2 4 5 10 12
2 5 9 10 12
3 4 5 9 11
2 5 7 8 11
3 6 8 11 12
4 5 7 8 9
2 6 8 9 10
2 3 6 7 10
2 5 6 10 12
4 8 9 10 11
5 6 7 9 10 11 12
2 3 9
2 3 6 7 8 9 12

LIST OF REFERENCES

A. Viterbi, A.J., Principles of Coherent Communications, McGraw-Hill, 1966.

B. Peterson, W.W., Error-Correcting Codes, MIT Press, 1961.

C. Advisory Group for Aerospace Research and Development, Spread Spectrum Communications, 1973.

INITIAL DISTRIBUTION LIST

		No. Copies
1.	Library, Code 0212 Naval Postgraduate School Monterey, California 93940	2
2.	Associate Professor J.E. Ohlson, Code 52OL Department of Electrical Engineering Naval Postgraduate School Monterey, California 93940	5
3.	Department Chairman, Code 52 Department of Electrical Engineering Naval Postgraduate School Monterey, California 93940	1
4.	Associate Professor Glen Myers, Code 52Mv Department of Electrical Engineering Naval Postgraduate School Monterey, California 93940	1
5.	Lieutenant Richard Pettus SMC 1061 Naval Postgraduate School Monterey, California 93940	1
6.	Lieutenant Sidney M. Skjei, Jr. USN NTSA Group 4401 Massachusetts Ave. (N.W.) Washington, D.C. 20390	3
7.	Defense Documentation Center Cameron Station Alexandria, Virginia 22314	2